ACUMOS SUPER VGA VIDEO CONTROLLER
AVGA2

OVERVIEW

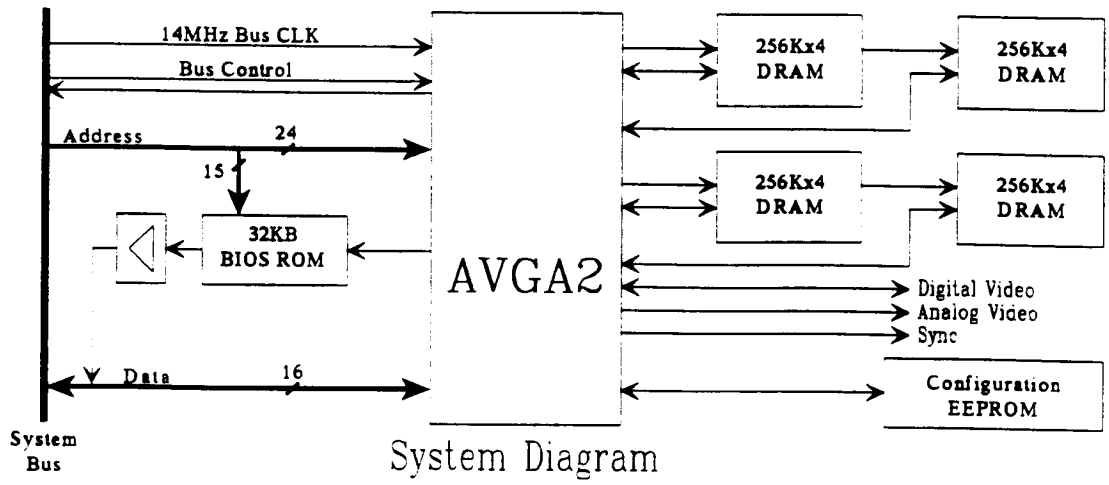
The AVGA2 Video Controller is the most highly integrated 512K VGA controller available today. Incorporating a built-in video DAC, Clock Synthesizer, and all System Bus and Feature Connector interface support, the AVGA2 requires only the addition of DRAMs to complete the video system. Optimized DRAM timing, 16-bit interface and an advanced write buffer provides high-performance memory access. A hardware graphics cursor improves the performance and appearance of graphical user interfaces such as Microsoft Windows.

FEATURES

- Full IBM®VGA compatibility in a 144-pin Plastic Quad Flat Pack (PQFP) package.
- Built-in video DAC. The video outputs connect directly to analog displays.
- Built-in monitor type detection circuit.
- Four internal memory clocks available. (37.58, 41.16, 44.74 or 50.11 MHz)
- Programmable internal video clocks at up to 75 MHz
- Connects directly to the Micro Channel™ or PC/XT/AT system bus.
- Supports 16-bit data for I/O, display memory, and BIOS ROM.
- Supports two or four 256K x 4 DRAM, or one 256K x 16 DRAM
- Choice of two DRAM timings (high-performance & standard)
- Write cycles to display memory are optimized by combining a memory write buffer and zero wait state (AT Bus) request capability.
- Internal asynchronous display data FIFO allows the system optimum access to the memory.
- Supports EEPROM for (switchless) configuration data.
- 132-column alphanumeric mode on all monitors.
- 16-color Graphics Mode at 800x600
- Graphics Cursor; 32x32 pixel, Windows compatible

With four DRAM (512K memory):

- 2X Performance improvement over two DRAM configuration
- 256-color performance enhancements for Windows 3.0
- 256-color Graphics Modes at up to 800 x 600 resolution.
- 16-color Graphics Mode at 1024x768 (interlaced or non-interlaced).



System Diagram

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DRAM support:

Two, 256Kx4; 256K bytes
MD(15:8), A(8:0), RASn, CASn, WE1n
MD(15:8) = Maps 0,1,2,3

Four, 256Kx4; 512K bytes
MD(15:0), A(8:0), RASn, CASn, WE1n, WE0n
MD(7:0) and WE0N = Maps 0,2
MD(15:8) and WE1N = Maps 1,3

One, 256Kx16; 512K bytes (two WE type)
MD(15:0), A(8:0), RASn, CASn, WE1n, WE0n
MD(7:0) and WE0N = Maps 0,2
MD(15:8) and WE1N = Maps 1,3

Default timing: for generic DRAMs
RAS high: 2.5 MCLK min
RAS low: 3.5 MCLK min
CAS cycle: 2 MCLK
Use MCLK=37.5 for 80ns, 41 or 45MHz for 70ns

High-performance DRAM timing: for DRAMs with better CAS cycle times
RAS high: 3 MCLK min
RAS low: 4 MCLK min
CAS cycle: 2 MCLK
Use MCLK=45Mhz for 80ns, 50MHz for 70ns

DRAM Refresh is CAS-before-RAS.

MCLK options:

CF(10)	CF(9)	MCLK value
0	0	50.11363 MHz
0	1	44.74431 MHz
1	0	41.16477 MHz
1	1	37.58523 MHz

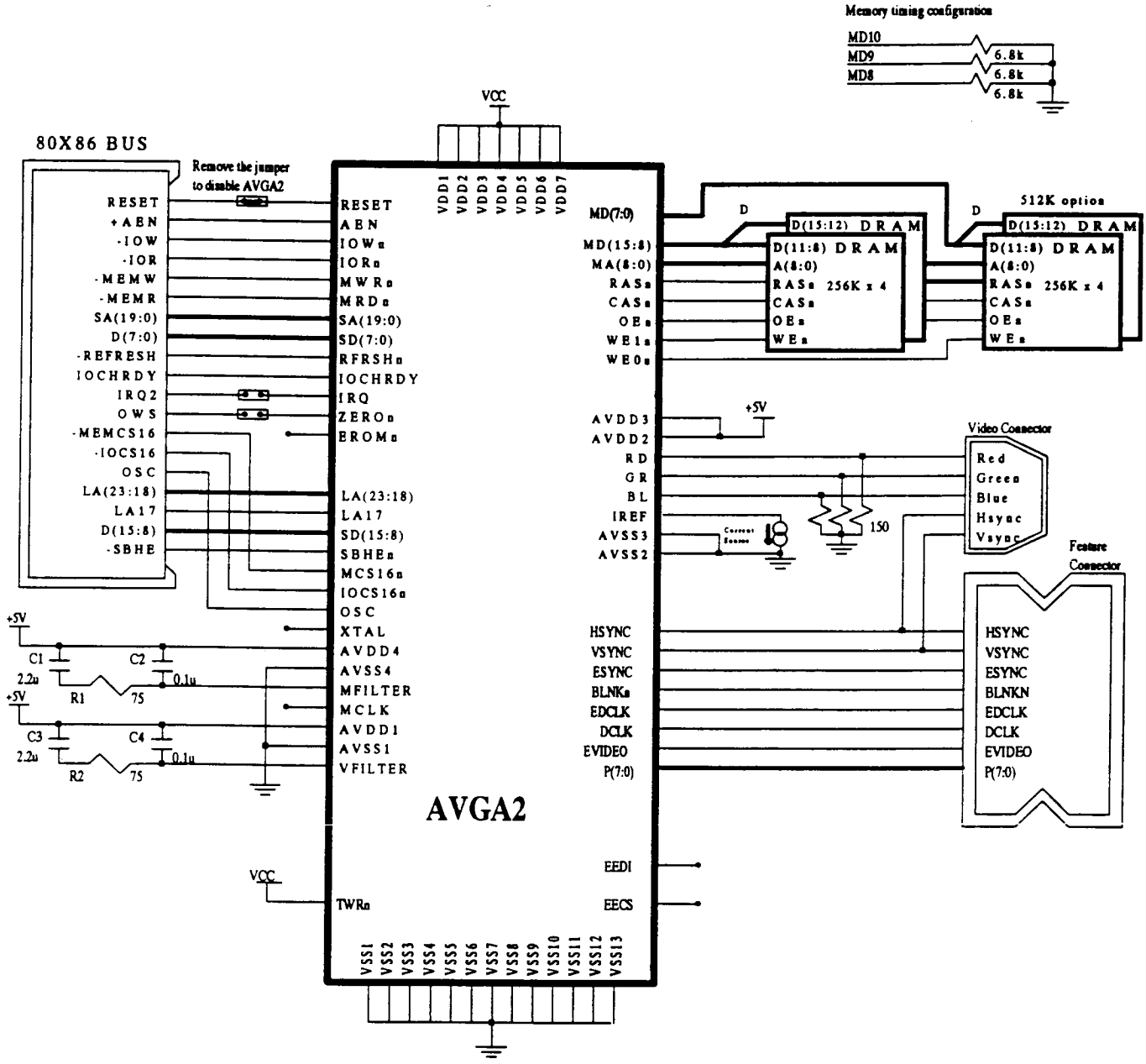
Video Clock Support

All four VCLK values are programmable, the power-on default values are:
VCLK0 = 25.1802 MHz (Standard VGA graphics)
VCLK1 = 28.3251 MHz (Standard VGA text)
VCLK2 = 41.1648 MHz (132 column text, PS/2 monitors)
VCLK3 = 36.0818 MHz (800 x 600, 56Hz)

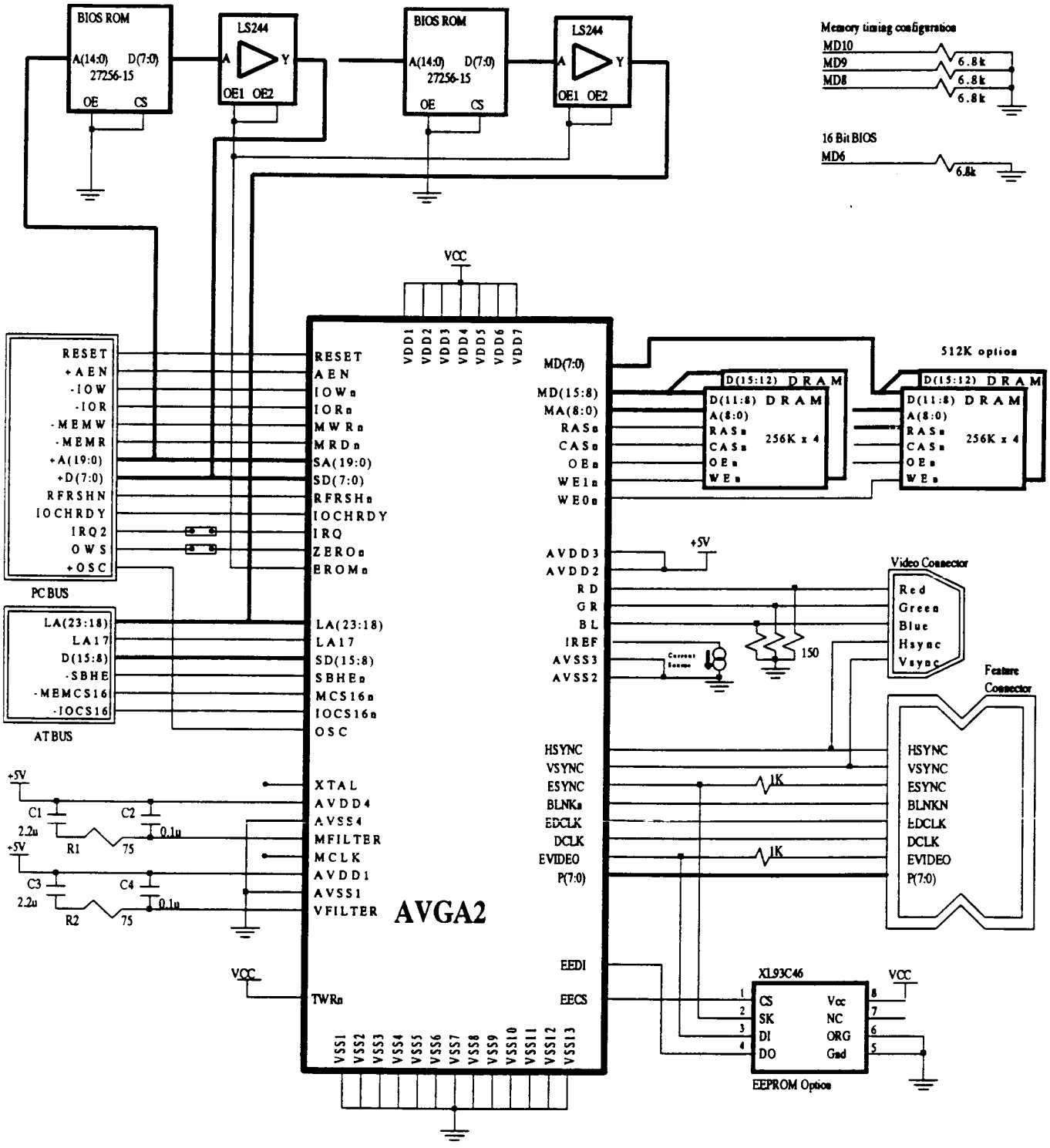
Other available frequencies (VCLK3):

31.193 (640x480, 72Hz)	50.113 (800x600, 72Hz)
39.992 (800x600, 60Hz)	64.982 (1024 x 768, 60Hz, non-interlaced)
44.907 (1024x768, interlaced)	75.169 (1024 x 768, 70Hz, non-interlaced)

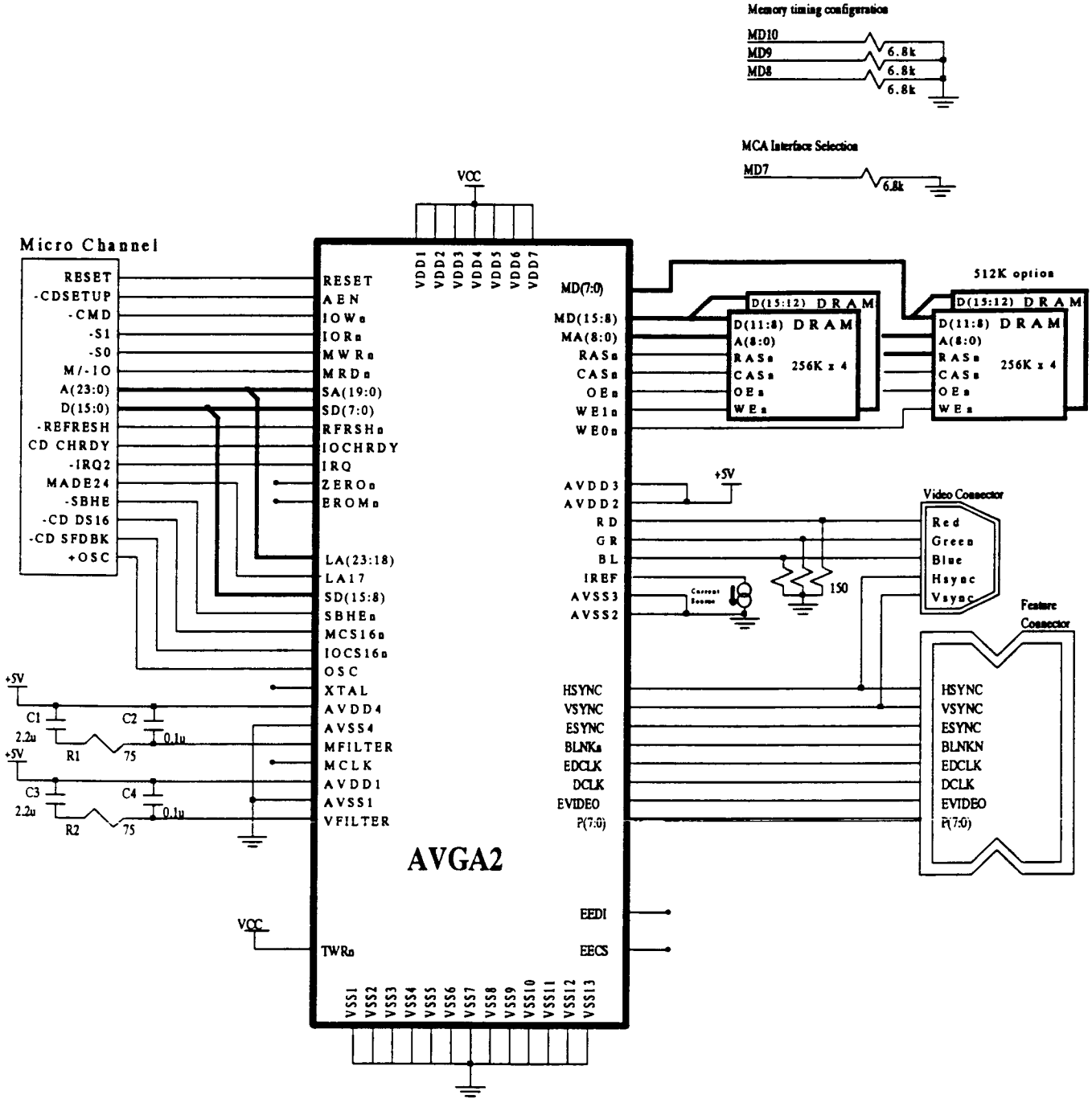
NOTE: Only those frequencies listed above will be guaranteed by testing. All other intermediate frequencies will not be tested.



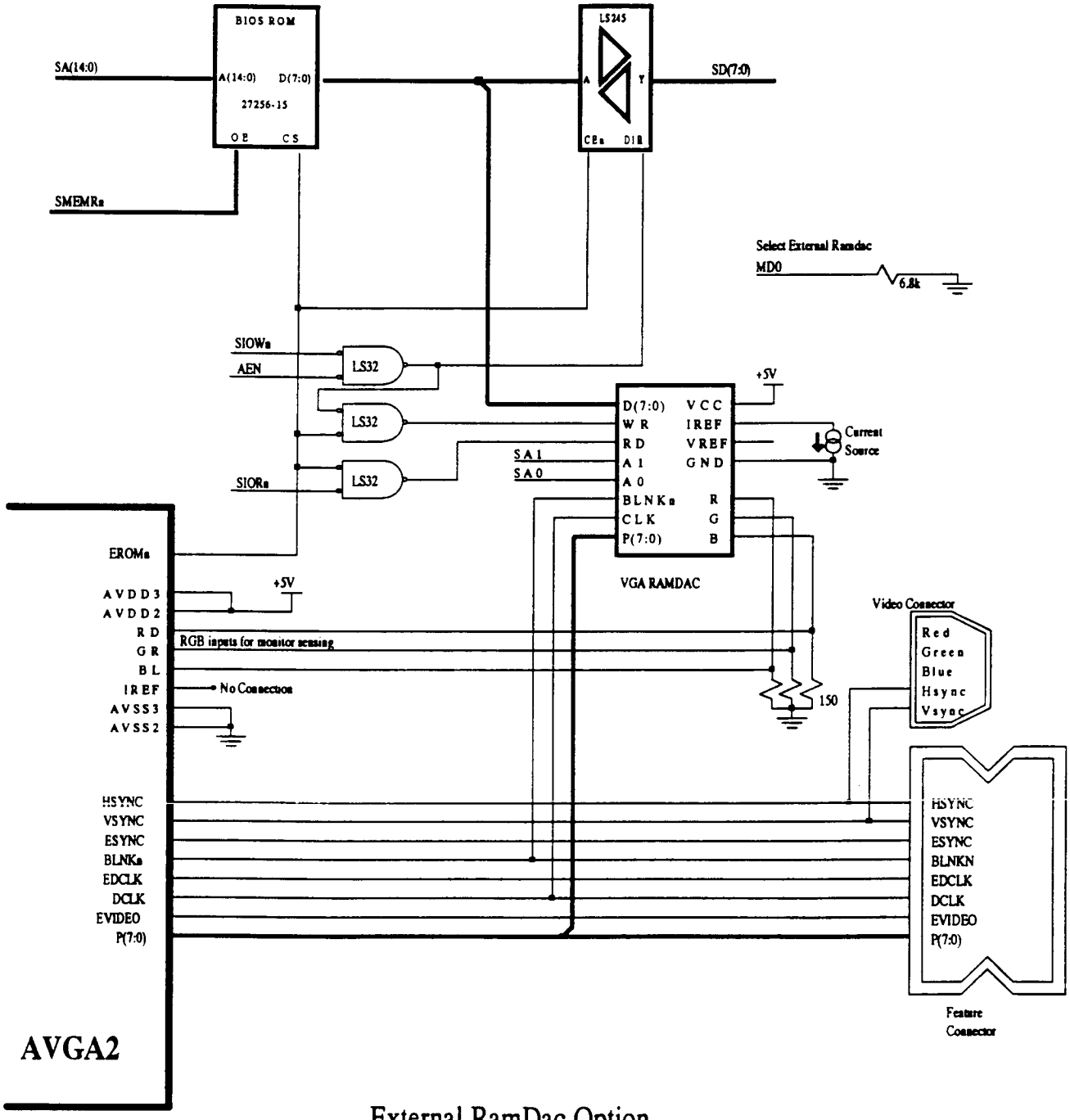
AT Mother-board Implementation



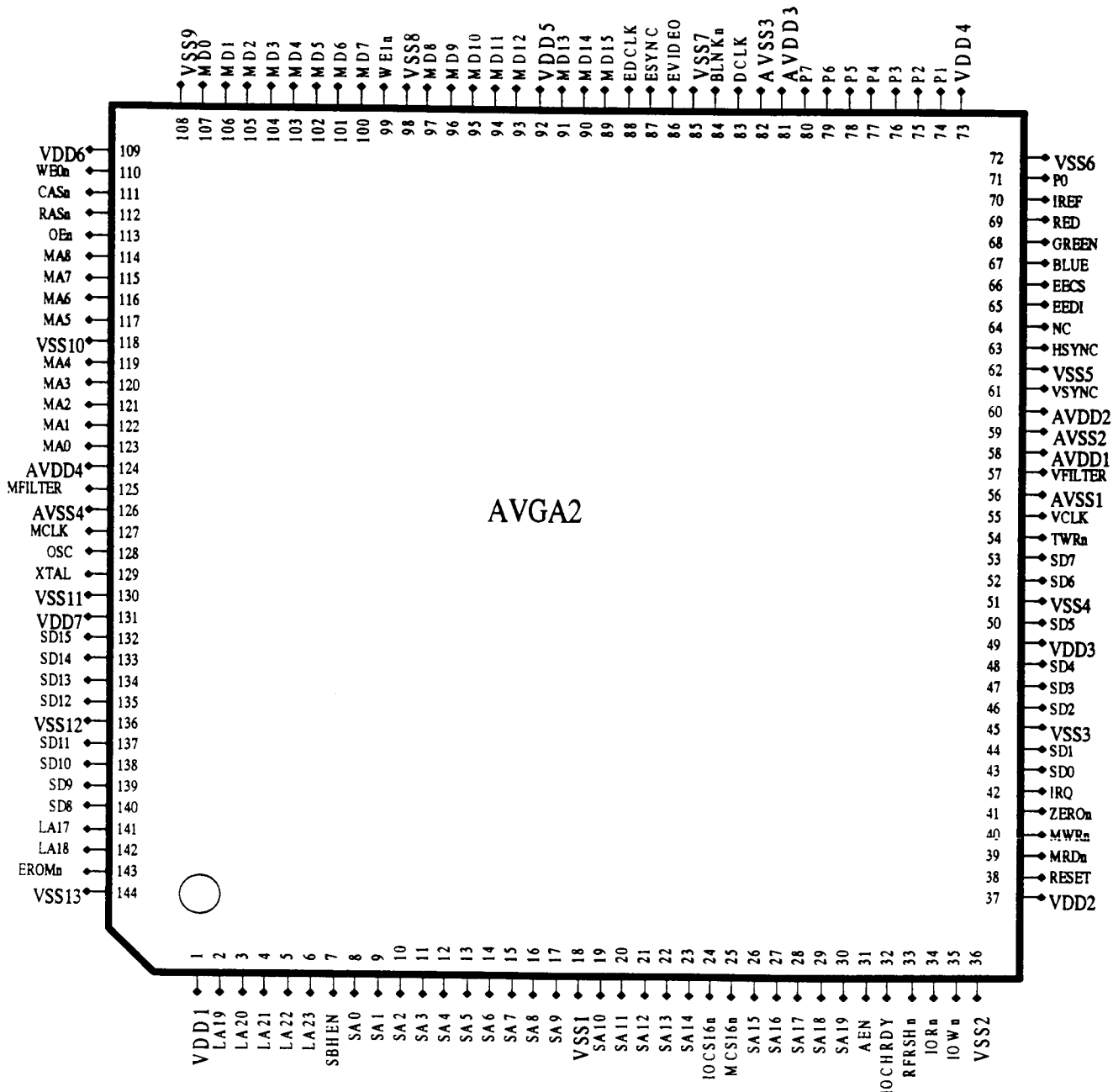
Typical PC/AT add-in 16 bit BIOS



MCA Implementation



External RamDac Option



144 PIN PQFP pinout

Pin Description Table

Pin Name	Pin #	Pin Type	Internal[0] pull-up	OUTPUT CURRENT (mA MIN) Ioh (Voh= 2.4V)	Iol (Vol=0.4V)	Load (pf Max)	Signal Interface/Description AT Bus	Micro Channel
SYSTEM BUS INTERFACE								
RESET	38	IN	o				RESET	CHRESET
LA 23	6	IN	o				LA 23	A 23
LA 22	5	IN	o				LA 22	A 22
LA 21	4	IN	o				LA 21	A 21
LA 20	3	IN	o				LA 20	A 20
LA 19	2	IN	o				LA 19	not used
LA 18	142	IN	o				LA 18	not used
LA 17	141	IN	o				LA 17	MADE24
SA 19	30	IN					SA 19	A 19
SA 18	29	IN					SA 18	A 18
SA 17	28	IN					SA 17	A 17
SA 16	27	IN					SA 16	A 16
SA 15	26	IN					SA 15	A 15
SA 14	23	IN					SA 14	A 14
SA 13	22	IN					SA 13	A 13
SA 12	21	IN					SA 12	A 12
SA 11	20	IN					SA 11	A 11
SA 10	19	IN					SA 10	A 10
SA 9	17	IN					SA 9	A 9
SA 8	16	IN					SA 8	A 8
SA 7	15	IN					SA 7	A 7
SA 6	14	IN					SA 6	A 6
SA 5	13	IN					SA 5	A 5
SA 4	12	IN					SA 4	A 4
SA 3	11	IN					SA 3	A 3
SA 2	10	IN					SA 2	A 2
SA 1	9	IN					SA 1	A 1
SA 0	8	IN					SA 0	A 0
SD 15	132	IN/OUT	o	-3[1]	12[2]	240	SD 15	D 15
SD 14	133	IN/OUT	o	-3	12	240	SD 14	D 14
SD 13	134	IN/OUT	o	-3	12	240	SD 13	D 13
SD 12	135	IN/OUT	o	-3	12	240	SD 12	D 12
SD 11	137	IN/OUT	o	-3	12	240	SD 11	D 11
SD 10	138	IN/OUT	o	-3	12	240	SD 10	D 10
SD 9	139	IN/OUT	o	-3	12	240	SD 9	D 9
SD 8	140	IN/OUT	o	-3	12	240	SD 8	D 8
SD 7	53	IN/OUT	o	-3	12	240	SD 7	D 7
SD 6	52	IN/OUT	o	-3	12	240	SD 6	D 6
SD 5	50	IN/OUT	o	-3	12	240	SD 5	D 5
SD 4	48	IN/OUT	o	-3	12	240	SD 4	D 4
SD 3	47	IN/OUT	o	-3	12	240	SD 3	D 3
SD 2	46	IN/OUT	o	-3	12	240	SD 2	D 2
SD 1	44	IN/OUT	o	-3	12	240	SD 1	D 1
SD 0	43	IN/OUT	o	-3	12	240	SD 0	D 0
SBHEN	7	IN	o				SBHE	-SBHE
RFRSHN	33	IN					-REFRESH	-REFRESH
AEN	31	IN					AEN	-CD SETUP(n)
MWRN	40	IN					-SMEMW	-S0
MRDN	39	IN					-SMEMR	M/-IO
IOWN	35	IN					-SIOW	-CMD
IORN	34	IN					-SIOR	-S1
IOCHRDY	32	OUT		-3	12	200	IOCHRDY	CD CHRDY(n)
IOCS16N	24	OUT		-3	20	200	-IO CS16	-CD SFDBK(n)
MCS16N	25	OUT		-3	20	200	-MEM CS16	-CD DS 16(n)
IRQ	42	OUT		-3	12	200	IRQ	-IRQ
ZERON	41	OUT		--	20	200	0WS	not used

[0](250K Ohm +/- 50%) [1] (-15 mA @ 2.0V) [2] (24 mA @ 0.5V)

Pin Description Table (Continued)

Pin Name	Pin #	Pin Type	Internal[0] pull-up	OUTPUT CURRENT (mA MIN) Ioh (Voh= 2.4V)	Iol (Vol=0.4V)	Load (pf Max)	Signal Description
CLOCK SYNTHESIZER							
OSC	128	TTL In					Ref Clock Input to Synthesizer
XTAL	129	Analog Out					Use for optional 14.31818 Xtal
MFILTER	125	Analog In/Out					MCLK VCO phase comparator
VFILTER	57	Analog In/Out					VCLK VCO phase comparator
MCLK	127	TTL In/Out					Opt. external MCLK input
VIDEO INTERFACE							
VSYNC	61	TTL Out (Tri-state)		-12	12	50	Vertical Sync
HSYNC	63	TTL Out (Tri-state)		-12	12	50	Horizontal Sync
BLNKN	84	TTL In/Out		-12	12	50	Blanking
ESYNC	87	TTL In	o	-12	12	50	Enable Sync
P7	80	TTL In/Out		-12	12	50	Pixel Data Bit 7
P6	79	TTL In/Out		-12	12	50	Pixel Data Bit 6
P5	78	TTL In/Out		-12	12	50	Pixel Data Bit 5
P4	77	TTL In/Out		-12	12	50	Pixel Data Bit 4
P3	76	TTL In/Out		-12	12	50	Pixel Data Bit 3
P2	75	TTL In/Out		-12	12	50	Pixel Data Bit 2
P1	74	TTL In/Out		-12	12	50	Pixel Data Bit 1
P0	71	TTL In/Out		-12	12	50	Pixel Data Bit 0
DCLK	83	TTL In/Out		-12	12	50	DAC Clock
EVIDEO	86	TTL In	o				Enable Video
EDCLK	88	TTL In	o				Enable DAC Clock
VCLK	55	TTL In					Optional External VCLK
RED	69	Analog In/Out					Red Video Output
GREEN	68	Analog In/Out					GreenVideo Output
BLUE	67	Analog In/Out					BlueVideo Output
IREF	70	Analog In					DAC Current Reference
DRAM INTERFACE							
RASN	112	TTL Out		-12	12	35	Row Address Strobe
CASN	111	TTL Out		-12	12	35	Column Address Strobe
OEN	113	TTL Out		-12	12	35	Output Enable
WE1N	99	TTL Out		-12	12	35	Write Enable for MD(15:8)
WE0N	110	TTL Out		-12	12	35	Write Enable for MD(7:0)
MA 8	114	TTL Out		-12	12	35	Memory Address 8
MA 7	115	TTL Out		-12	12	35	Memory Address 7
MA 6	116	TTL Out		-12	12	35	Memory Address 6
MA 5	117	TTL Out		-12	12	35	Memory Address 5
MA 4	119	TTL Out		-12	12	35	Memory Address 4
MA 3	120	TTL Out		-12	12	35	Memory Address 3
MA 2	121	TTL Out		-12	12	35	Memory Address 2
MA 1	122	TTL Out		-12	12	35	Memory Address 1
MA 0	123	TTL Out		-12	12	35	Memory Address 0
MD 15	89	TTL In/Out	o	-12	12	35	Memory Data 15
MD 14	90	TTL In/Out	o	-12	12	35	Memory Data 14
MD 13	91	TTL In/Out	o	-12	12	35	Memory Data 13
MD 12	93	TTL In/Out	o	-12	12	35	Memory Data 12
MD 11	94	TTL In/Out	o	-12	12	35	Memory Data 11
MD 10	95	TTL In/Out	o	-12	12	35	Memory Data 10
MD 9	96	TTL In/Out	o	-12	12	35	Memory Data 9
MD 8	97	TTL In/Out	o	-12	12	35	Memory Data 8
MD 7	100	TTL In/Out	o	-12	12	35	Memory Data 7
MD 6	101	TTL In/Out	o	-12	12	35	Memory Data 6
MD 5	102	TTL In/Out	o	-12	12	35	Memory Data 5
MD 4	103	TTL In/Out	o	-12	12	35	Memory Data 4
MD 3	104	TTL In/Out	o	-12	12	35	Memory Data 3
MD 2	105	TTL In/Out	o	-12	12	35	Memory Data 2
MD 1	106	TTL In/Out	o	-12	12	35	Memory Data 1
MD 0	107	TTL In/Out	o	-12	12	35	Memory Data 0

Pin Description Table (Continued)

Pin Name	Pin #	Pin Type	OUTPUT CURRENT (mA MIN) Internal pull-up	Ioh (Voh= 2.4V)	Iol (Vol=0.4V)	Load (pf Max)	Signal Description
BIOS ROM SUPPORT							
EROMN	143	TTL Out		-12	12	35	Enable BIOS ROM
TEST							
TWRN	54	TTL In	o				Test Latch load enable
EEPROM SUPPORT							
EECS	66	TTL Out		-12	12	35	EEPROM chip select
EEDI	65	TTL In		-12	12	35	EEPROM data out (KALN)
NC	64	TTL Out		-12	12	35	No connection

POWER/GROUND

Pin Name	Pin Number(s)	Supply	Circuit Section
VDD1	1	+5V	LOGIC
VDD2	37	+5V	LOGIC
VDD3	49	+5V	LOGIC
VDD4	73	+5V	LOGIC
VDD5	92	+5V	LOGIC
VDD6	109	GND	LOGIC
VDD7	131	GND	LOGIC
VSS1	18	GND	LOGIC
VSS2	36	GND	LOGIC
VSS3	45	GND	LOGIC
VSS4	51	GND	LOGIC
VSS5	62	GND	LOGIC
VSS6	72	GND	LOGIC
VSS7	85	GND	LOGIC
VSS8	98	GND	LOGIC
VSS9	108	GND	LOGIC
VSS10	118	GND	LOGIC
VSS11	130	GND	LOGIC
VSS12	136	GND	LOGIC
VSS13	144	GND	LOGIC
AVDD2	60	+5V	VIDEO DAC
AVDD3	81	+5V	VIDEO DAC
AVSS2	59	GND	VIDEO DAC
AVSS3	82	GND	VIDEO DAC
AVDD1	58	+5V	VCLK VCO
AVSS1	56	GND	VCLK VCO
AVDD4	124	+5V	MCLK VCO
AVSS4	126	GND	MCLK VCO

Detailed Pin Descriptions - System Bus Interface

AEN

PC/AT BUS: Address Enable. When this input signal is high during a bus cycle, the System's DMA Controller has control of the System's Address, Data, and Control lines. If this pin is high during an I/O or Memory transfer cycle to a valid AVGA2 address, the AVGA2 responds to Memory cycles only; if low, the AVGA2 responds to both I/O and Memory cycles.

Micro Channel: -Card Setup. When this signal is driven low, the AVGA2 is placed in Setup Mode and maps in the POS (Programmable Option Select) Register 2 at I/O address 102H.
The AVGA2 then responds only to I/O read/write accesses to port 102; it does not respond to Video Memory access.
This signal may be supplied to the AVGA2 either latched or unlatched, because the signal is latched internally while input -CMD (pin IOWN) is low. For a motherboard-based VGA design, this signal would ordinarily be supplied from bit 5 of the System Board Enable/Setup Register at I/O address 094H.

IOCHRDY

PC/AT BUS: I/O Channel Ready. This output, by going low, requests that Video Memory access cycles be lengthened until it is driven high. This tri-state output floats whenever the AVGA2 is not participating in a Video Memory access cycle. This pin remains tri-stated off during Video BIOS ROM accesses and all I/O cycles.

In Memory read cycles, the leading edge of the active low input MRDN always causes this output to go low. This output is clocked high when the AVGA2 has completed the memory data transfer. The output remains high until MRDN going inactive causes it to float.

In Memory write cycles, the AVGA2 can drive this pin high immediately, by the leading edge of active low input MWRN. The reason is that the AVGA2's MEMORY WRITE DATA FIFO stores the data being written, releases the Processor by driving this pin high, then performs the write cycle later. If the FIFO is not ready for more data at the start of a Memory write cycle, then this pin is driven low by the leading edge of MWRN.

Micro Channel: Channel Ready. This output, by going low, requests that Video Memory access cycles be lengthened until it is driven high. This pin is not tri-state, and remains high when the AVGA2 is not responding to a memory cycle. This pin remains high during Video BIOS ROM accesses and all I/O cycles.

In Memory read cycles, a valid Address decode and valid Status always causes this output to go low. This output is clocked high when the AVGA2 has completed the memory access. The Address decode is generated from Micro Channel signals A(23:0), MADE24, -REFRESH, and M/-IO; the Status is a decode of -S0 and -S1.
In Memory write cycles, this pin can be driven high immediately after a valid decode of Address and Status.

Detailed Pin Descriptions - System Bus Interface

IOCS16N

AT BUS: -I/O 16 bit Chip Select. This open-collector output pin signals the System Processor that the present cycle is a 16-bit I/O cycle. The signal is generated from an address decode of inputs SA(15:0) and AEN, for the following I/O ports:

3C4,3C5	(SEQUENCER)
3CE,3CF	(GRAPHICS CONTROLLER)
3B4/3D4,3B5/3D5	(CRT CONTROLLER)
3BA/3DA	(INPUT STATUS REGISTER 1)

Micro Channel: -Card Selected Feedback. This pin is driven low by a valid Address decode whenever the System Processor addresses I/O ports or Memory segments where the AVGA2 is mapped in. The Address decode is generated from Micro Channel signals A(23:0), MADE24, -REFRESH, and M/-IO. The memory segment addressing range includes the Video BIOS ROM only if it is 16 bits, indicated by setting Configuration Register bit CF(6)=0; if CF(6)=1, then this pin remains high while accessing the BIOS ROM. Accessing I/O ports 102H or 3C3H does not cause this pin to go low, although the AVGA2 contains these registers.

This pin remains high while the AVGA2 is in Setup Mode (see pin AEN), regardless of the address.

IORN

PC/AT BUS: -I/O Read. This active low input causes the AVGA2 to drive I/O port data onto the System Data Bus during an I/O read bus cycle.

Micro Channel: -Status Bit 1. This input, and two other inputs -Status Bit 0 (MWRN) and M/-IO (MRDN), are fully decoded and latched by -CMD (pin IOWN) low. The resulting latched decode determines the type of channel cycle, as given in the following table:

M/-IO	-S0	-S1	Cycle Type
0	0	1	I/O write
0	1	0	I/O read
1	0	1	Memory write
1	1	0	Memory read
X	0	0	none
X	1	1	none

IOWN

PC/AT BUS: -I/O Write. This active low input causes the AVGA2 to transfer data from the System Data Bus into a register during an I/O write bus cycle. Data is written to a register by the trailing edge of this signal.

Micro Channel: -Command. This active low input signal is used to latch the System Address and Status into transparent latches. The latched Address and Status decode is gated with this signal to provide timing control during read/write bus cycles. During read cycles, the AVGA2 drives valid data onto the System Data Bus before the trailing edge of this signal. During write cycles, data written to Video Memory is expected to be valid throughout the interval when this input is low; data is written to I/O ports by the trailing edge of this signal.

Detailed Pin Descriptions - System Bus Interface

IRQ

PC/AT BUS: Interrupt Request. A low to high transition on this output indicates that the AVGA2's CRT Display timing has reached the end of the active display frame, at the start of the bottom screen border. This signal is ordinarily unused in PC/AT-based VGA add-in boards. Connecting this pin to one of the System's IRQ lines through a jumper block is recommended, to allow its possible use. This pin is a tri-state buffer, enabled by CRTC Register 11H bit 5=0.

Micro Channel: -Interrupt Request. A high impedance to low transition on this open collector output indicates that the AVGA2's CRT Display timing has reached the end of the active display frame, at the start of the bottom screen border. This pin is not driven high. Transitions on this output are enabled only if CRTC Register 11H bit 5=0 and POS Register 2 (102H) bit 0=1.

LA 17

AT BUS: Latchable Address 17. The combined decode of this input signal with inputs LA(23:18) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of LA(23:18), this pin, and SA(16:15).

Micro Channel: Memory Address Enable 24. This input signal is latched by a low -CMD (IOWN) signal and must be high during a Memory cycle in order for the AVGA2 to participate in the cycle.

LA 19:18

AT BUS: Latchable Addresses 19 & 18. The combined decode of these input signals with inputs LA(23:20) and LA(17) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of LA(23:20), these pins, LA(17), and SA(16:15).

Micro Channel: Not used. These inputs have internal pull-up resistors and may be left to float.

LA 23:20

AT BUS: Latchable Addresses 23-20. The combined decode of these input signals with inputs LA(19:17) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of these pins, LA(19:17), and SA(16:15).

Micro Channel: Address Bits 23-20. These address inputs are latched by a low -CMD (IOWN) signal and must all be zero during a Memory cycle in order for the AVGA2 to participate in the cycle.

Detailed Pin Descriptions - System Bus Interface

MCS16N

AT BUS: -MEM 16 Chip Select. This open-collector output requests the System Processor to make the present cycle a 16-bit Memory cycle. This signal is generated either from an address decode of inputs LA(23:17) during Video Memory access, or from an address decode of LA(23:17) and SA(16:15) during BIOS ROM access. In both cases, other conditions qualify the 16-bit requests. Video memory 16-bit cycles are enabled by the AVGA2 if no other Video Controller is detected in the System, in order to prevent requesting 16-bit cycles while the other Video Controller's memory is accessed. BIOS ROM 16-bit Memory cycles are enabled only if Configuration Register bit CF(6)=0 (BIOS ROM is 16 bits).

Although delays introduced into the latched System Addresses SA(16:15) by the System commonly make these signals unreliable for generating 16-bit memory requests, the AVGA2 incorporates an especially high speed signal path design from these inputs to the MCS16N output buffer, to achieve reliability.

Micro Channel: -Card Data Size 16. This totem pole output requests the System Processor to make the present Memory or I/O cycle a 16-bit cycle.

This signal is generated from the combined decode of unlatched Micro Channel signals MADE24, -REFRESH, M/-IO, and inputs A(23:0) which define the addressing range: A(23:15) for Video Memory, and A(23:11) for the BIOS ROM. This output is also driven low while accessing the same 16-bit I/O ports listed previously in the description of pin IOCS16N's function in the AT BUS. The signal is generated from the combined decode of unlatched M/-IO and A(15:1).

MRDN

PC/AT BUS: -Memory Read. This active low input causes the AVGA2 to drive Video Memory data onto the System Data Bus during a Video Memory read cycle. The signal should be connected to the AT BUS signal -SMEMR, active during memory read cycles within the lower 1 Mb of System Address space.

This input signal also strobes the output EROMN, which controls external bus buffer(s) driving BIOS ROM data onto the System Data Bus.

Micro Channel: Memory/-Input Output. This input, and two other inputs -Status Bit 0 (MWRN) and -Status Bit 1 (IORN), are fully decoded and latched by the leading edge of -CMD (IOWN). The resulting latched decode determines the type of channel cycle, as shown in the table under the description of pin IORN.

MWRN

PC/AT BUS: -Memory Write. This active low input causes the AVGA2 to write data from the System Data Bus into Video Memory. The signal should be connected to the AT BUS signal -SMEMW, active during memory write cycles within the lower 1 Mb of System Address space.

Micro Channel: -Status Bit 0. This input, and two other inputs -Status Bit 1 (IORN) and M/-IO (MRDN), are fully decoded and latched by the leading edge of -CMD (IOWN). The resulting latched decode determines the type of channel cycle, as shown in the table under the description of pin IORN.

Detailed Pin Descriptions - System Bus Interface

RESET
This active high input initializes the AVGA2. The high to low transition of this input loads the Configuration Register CF(7:0) with data present on the MD(7:0) pins, determined by internal pull-up resistors and external, optional pull-downs.

RFRSHN
PC/AT BUS: -Refresh. This input signal must be high during a Video Memory read cycle in order for the AVGA2 to participate in the cycle.

Micro Channel: -Refresh. This input signal is latched by a low -CMD (IOWN) signal and must be high during a Video Memory cycle in order for the AVGA2 to participate in the cycle.

SA 19:0
System Address Bits SA(19:0). These address inputs are decoded to select Memory and I/O during read/write access cycles. Video Memory is selected by decoding SA(19:15), and the BIOS ROM by decoding SA(19:11). All I/O ports are selected by decoding SA(15:0) except POS Register 2, which is selected by decoding SA(2:0).

In Micro Channel operation, these address inputs are transferred into transparent latches by a low IOWN (-CMD) signal and therefore may change state while IOWN is low. In PC/AT BUS operation, however, these address inputs are not latched and must remain valid during the data access cycle.

Inputs SA(12:2) and input TWRN also provide access to eight, 8-bit Test Registers used for chip manufacturing test (see the description of pin TWRN).

SBHEN
System Byte High Enable. This active low input enables data to be transferred across System Data Bus pins SD(15:8). This input and pin SA(0) are decoded to distinguish between low byte and high byte data transfers. This input should be connected to the AT BUS or Micro Channel signal -SBHE. The signal is internally latched in Micro Channel operation, by input IOWN (-CMD) low.

This pin has an internal pull-up resistor which ensures that this input is forced inactive if an AVGA2 is installed in an 8-bit card slot. The AVGA2 traps any high to low level transition of this input after RESET has been asserted, to determine whether it is installed in a 16-bit card slot and properly control output ZERON.

Detailed Pin Descriptions - System Bus Interface

SD 15:8
System Data Bus bits 15-8. These bi-directional pins transfer I/O and Video Memory data during 16-bit bus cycles. During 16-bit read cycles, input signal SBHEN=0 (internally latched in Micro Channel operation) enables these output buffers. These pins have internal pull-up resistors, in order to reduce internal power whenever these inputs are allowed to float, as in an 8-bit System.

SD 7:0
System Data Bus bits 7-0. These bi-directional pins transfer data during all I/O and Video Memory accesses. During read operations, all output buffers are enabled except in the special case of reading (Micro Channel operation only) the VGA Enable Register at I/O address 3C3H. Only bit 0 of this register is driven onto SD(0) by the AVGA2.

ZERON
AT BUS: Zero Wait State. This open collector output pin is driven low to signal the System Processor that it can complete the present bus cycle without inserting any additional wait states.

The AVGA2 drives this pin low in order to shorten Video Memory read/write cycles or BIOS ROM read cycles; this output remains inactive during I/O access cycles. ZERON is driven active during all Video Memory access cycles, but it can go active during BIOS ROM read cycles only if Configuration Register bit CF(1) has been cleared to 0.

In Video Memory read/write cycles, ZERON is driven low by output IOCHRDY being driven high, signalling the Processor that data transfer is complete and that no additional wait states are required. During some write cycles, in which the AVGA2 stores data temporarily in the MEMORY WRITE DATA FIFO, ZERON is driven low almost immediately by input MWRN going low, because IOCHRDY remains high. ZERON goes low while accessing any odd-addressed byte of Video Memory, and also while reading any even-addressed byte only if no second installed card has been detected and the AVGA2 is installed in a 16-bit card slot (refer to the description of input SBHEN).

During a BIOS ROM read cycle, ZERON is driven low by input MRDN being driven low. It remains low until MRDN is driven high. ZERON goes low while reading any odd-addressed byte of the BIOS ROM, and also while reading any even-addressed byte only if Configuration Register bit CF(6)=0 and the AVGA2 is installed in a 16-bit card slot (refer to the description of input SBHEN). Use of ZERON typically results in reduction of BIOS ROM read cycles from 3 to 2 processor clock cycles (one Send-Status [Ts] and one Command [Tc] cycle).

Micro Channel: This output is disabled and remains high impedance.

Detailed Pin Descriptions - Clock Synthesizer

OSC

This TTL input pin is the reference clock input of the CLOCK SYNTHESIZER. It is normally driven by the clock signal; OSC, supplied by both the AT BUS and the MICRO CHANNEL System Bus Interfaces. Alternatively, this input can be driven by a 14.31818 MHz CRYSTAL, connected across this pin and the XTAL pin. It requires an input frequency of 14.31818 MHz +/- 0.01%, with a duty cycle of 50% +/- 10 %. The internal clock synthesizer uses this input signal in to generate Memory Timing Clock (MCLK) and Video Dot Clock (VCLK).

XTAL

This analog input pin is provided to facilitate the use of a discrete crystal in the absence of a 14.31818 MHz. signal from the system bus. The input clock of the CLOCK SYNTHESIZER can be supplied by a 14.31818 MHz crystal, connected across this pin and the OSC pin.

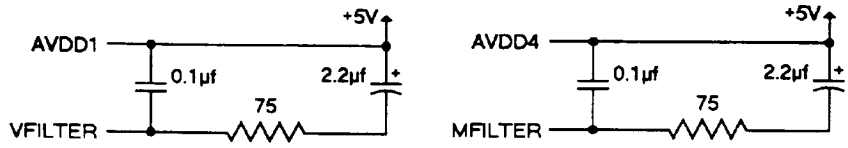
MFILTER

The VCO which generates the Memory Timing Clock (MCLK) requires a filter network to be connected between this pin and the AVDD4 pin, as shown in the illustration below. This is an analog input/output pin.

VFILTER

The VCO which generates the Video Clock (VCLK) requires a filter network to be connected between this pin and the AVDD1 pin, as shown in the illustration below. This is an analog input/output pin.

Typical Filters:



MCLK

Normally, the CLOCK SYNTHESIZER generates the internal Memory Timing Clock, and this pin functions as a test output for monitoring the internal MCLK. This is a TTL input/output pin. The frequency of MCLK is determined by Configuration Register bits CF(10:9), as shown:

Config.	Frequency
CF(10:9)=11	37.585 MHz
CF(10:9)=10	41.164 MHz
CF(10:9)=01	44.744 MHz
CF(10:9)=00	50.113 MHz

Duty cycle: 50 +/- 10 %
Ioh = -12 mA min (Voh=2.4V)
Iol = 12 mA min (Vol=0.4V)
Load = 10 pf max

The CLOCK SYNTHESIZER's MCLK VCO can be disabled, however, by setting Configuration Register bit CF(4)=0, so that MCLK may be supplied by an external, TTL-level clock source.

Detailed Pin Descriptions - Video Interface

VSYNC
This signal is the vertical sync pulse driving the CRT display and also supplied externally to the FEATURE CONNECTOR.

HSYNC
This signal is the horizontal sync pulse driving the CRT display and also supplied externally to the FEATURE CONNECTOR.

BLNKN
The signal on this bi-directional pin is fed back into the BLANK input of the Video DAC. When low, this signal causes the output pins RED, GREEN,and BLUE to be 0 V. This pin is connected externally to the FEATURE CONNECTOR.

ESYNC
This pin controls the output buffer pins of VSYNC, HSYNC, and BLNKN; driving this pin low disables (floats) the outputs. This pin also provides the EEPROM data shift clock, SK, when configured by Sequencer Register 8.

P 7:0
The signals on these bi-directional pins are fed back into the PIXEL ADDRESS inputs of the Video DAC. These pins are connected externally to the FEATURE CONNECTOR.

The input pin EVIDEO controls the output buffers of these bi-directional pins. If EVIDEO is driven low, then these pins become inputs, and the Video DAC's PIXEL ADDRESS inputs can be driven externally by the FEATURE CONNECTOR. If EVIDEO is high, then these pins are driven internally by the AVGA2.

DCLK
The rising edge of this signal latches the values of P(7:0) and the BLNKN signal into the Video DAC. It is typically the same frequency as the internal VIDEO DOT CLOCK.

The input pin EDCLK controls the output buffer of this bi-directional pin. If EDCLK is driven low, then this pin becomes an input, and the VIDEO DAC's PIXEL CLOCK input can be driven externally by the Feature Connector. If EDCLK is high, then this pin is driven internally by the AVGA2.

EVIDEO
This pin controls the output buffers of pins P(7:0); EVIDEO=0 floats the outputs. This pin also provides the EEPRM data output when configured for EEPROM support by Sequencer Register 8.

EDCLK
This pin controls the output buffer of pin DCLK; EDCLK=0 floats the output. This pin also controls selection of the Video Dot Clock.

EECS
This pins provides the EEPROM chip select, CS, for the optional configuration EEPROM that may be used to store monitor timing options.

EEDI
This pin provides the EEPROM data input for the optional configuration EEPROM.

Detailed Pin Descriptions - Video Interface

VCLK

This input can be selected as the source of the Video Dot Clock, VCLK3 , if Configuration Register bit CF(5)=0 (External VCLK3). Otherwise it may be left unconnected.

RED, GREEN, BLUE

These pins are the outputs of three 6-bit DACs. Each DAC consists of 63 summed current sources. A 6-bit register value applied to the DAC input determines the number of current sources to be summed.

Full-scale output: 0.70V ±7% (Termination: 50 Ohms to VSS)

The full-scale output current (I_f) sourced by each pin is related to the DAC Reference Current (IREFpin) as follows:

$I_f = (63/30)$ xIREF

To maintain IBM VGA compatibility, each pin should be terminated to ground through a precision resistor, 150 Ohm ± 2%. Additional termination to ground through a 75 Ohm ± 2% resistor should produce a loaded output level of 0.7 V ±7%. Therefore, the full-scale output current is nominally 14 mA.

IREF

The current drawn from VDD through this pin determines the full-scale output current of each DAC. (See pins RED, GREEN, & BLUE).

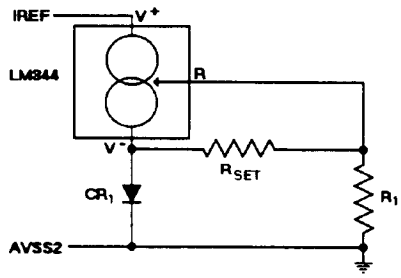
-3 mA ≤ I_{REF} ≤ -10 mA (@ VDD = 5.25 V)

This pin should be connected to a constant current source. An example of a current source based on the LM334, used in zero temperature coefficient mode, is given below. The nominal Iref is 6.67 mA, which produces a full-scale output current on RED, GREEN, & BLUE of 14 mA.

R_{SET}=20 Ohms +/-1%

R_1=200 Ohms +/-5%

CR_1= 1N4148 or equivalent



Notes:
R_{SET} determines IREF; R1 and CR1 provide temperature compensation.
The voltage (VSET) across R_{SET} varies according to temperature (T):
V_{SET} (mV) = 59 + 0.2T, 0° < T < 70° C

The current I_{SET} through resistor R_{SET} determines the output current: IREF = 2I_{SET}

Detailed Pin Descriptions - Dynamic RAM Interface

General
All outputs are generated synchronously from MCLK (Memory Timing Clock) timing. The output buffers can be turned off (high impedance), to facilitate board-level testing of the DRAMs (see the pin description of input TWRN).

RASN Row Address Strobe
The falling edge of this active low output coincides with output of a valid DRAM Row Address on pins MA(8:0).

CASN Column Address Strobe
The falling edge of this active low output coincides with output of a valid DRAM Column Address on pins MA(8:0). The rising edge latches data from the DRAM, on pins MD(7:0), into the AVGA2. CAS-before-RAS refresh is supported.

OEN Output Enable
Data from the DRAM is input to the AVGA2 through pins MD(7:0) while this signal and CASN are low.

WE1N Write Enable for MD(15:8)
Data is written to the DRAM through pins MD(15:8) by the falling edge of either this signal or CASN (Late/EarlyWrites).

WE0N Write Enable for MD(7:0)
Data is written to the DRAM through pins MD(7:0) by the falling edge of either this signal or CASN (Late/EarlyWrites).

MA(8:0) Memory Address (8:0)
These pins output addresses originating from the CRT Controller or System Address Bus.

MD(15:0) Memory Data 15:0
The System Processor reads and writes Video display data through these bi-directional pins; the CRT Controller sequentially reads data through them. The outputs float when input RESET is high.

If only two DRAMs are used (256Kb) then connect only pins MD(15:8). If four DRAMs are used (512Kb), use all 16 pins.

Also, these pins are inputs to the AVGA2 Configuration Register, which is loaded by the falling edge of RESET. Internal pull-ups provide a default value of FFH to be loaded. Configuration Register bits CF(7:0) are loaded from the correspondingly indexed pins MD(7:0).

Detailed Pin Descriptions - BIOS ROM Support

EROMN
This totem pole output controls the active low output enable inputs of up to two external 8-bit bus buffers, which drive BIOS ROM data onto the System Data Bus. This output is driven high by bringing the input RESET high.

This output can go active only if the System Processor is performing a Memory read cycle within the 32Kb segment from System Address C0000 through C7FFF. To maintain IBM® VGA compatibility, the 2Kb range from C6000 through C67FF is excluded from the address decode only if Configuration Register bit CF(2)=1, and the output remains inactive; otherwise, if bit CF(2)=0, then this output goes active while also addressing the 2Kb range. In PC/XT/AT operation, the address is decoded from SA(19:11); in Micro Channel operation, LA(23:20), SA(19:11), and LA(17) (MADE24) are decoded.

The output is strobed to go low by an active Memory read command asserted at an input pin. In PC/XT/AT operation, the strobing input signal is MRDN low; in Micro Channel operation, IOWN (-CMD) low.

Detailed Pin Descriptions - TEST Support

TWRN Test Latch Load Enable
This pin is used primarily for chip testing and must be driven high or allowed to float for normal operation of the chip. It can be used, however, in board-level testing, to disable (float) most of the AVGA2 outputs and drive them by a board tester.

This pin provides an active-low, load enable pulse to eight, 8-bit transparent latches which supply internal chip test mode functions. These latches are designated TESTREGISTERS TR0(7:0) through TR7(7:0). The address j of each latch TRj(7:0) is decoded from input pins SA(12:10), and the test data byte (7:0) written to the latch is obtained from input pins SA(9:2). All latch data bits are active high. All latches are cleared to 0 asynchronously by driving the RESET pin high, or allowing it to float.

Loading a test register consists of placing its address and test data onto pins SA(12:2), then bringing TWRN low. The test data is transferred to the latch outputs while TWRN remains low and remains latched after TWRN is returned high. While TWRN is low, the latch remains transparent; its outputs will follow any transitions on SA(9:2).

In order to disable the output buffers, set Test Register bit TR0(5)=1 by setting pins SA(12:2) = 020H and TWRN=0. To re-enable the output buffers, clear TR0(5) to 0, either by writing 0 to the register or by driving RESET high.

Setting TR0(5)=1 causes only the following outputs to be disabled (floating):

CASN	MD(15:0)
IOCHRDY	OEN
IOCS16N	RASN
IRQ	SD(15:0)
MA(8:0)	WE0N, WE1N
MCS16N	ZERON

STANDARD VGA REGISTERS

All of the AVGA2 registers summarized in the following table are equivalent to those found in the IBM VGA Display Adapter.

NAME	I/O Address	R/W	NOTES
Input Status Register 0	3C2	RO	
Miscellaneous Output Register	3C2	W	
	3CC	R	
Input Status Register 1	3BA/3DA	RO	
Feature Control Register	3BA/3DA	W	
	3CA	R	
VGA Enable Register	3C3	RW	Micro Channel only [CF(7)=0]
	46E8	WO	PC/XT/AT Bus only [CF(7)=1 and CF(3)=1]
	46E9	WO	PC/XT/AT Bus only [CF(7)=1 and CF(3)=0]
POS Register 2	102	RW	
Sequencer	3C4	RW	Index
	3C5	RW	Data registers 00 - 04
Graphics Controller	3CE	RW	Index
	3CF	RW	Data registers 00 - 08
CRT Controller	3B4/3D4	RW	Index
	3B5/3D5	RW	Data registers 00 - 18H
Attribute Controller	3C0	RW	Index
	3C0	W	Data registers 00 - 14H
	3C1	RO	Data registers 00 - 14H
Video DAC	3C6	RW	Pixel Mask Register
	3C7	WO	Pixel Address Register (read mode)
	3C7	RO	DAC State Register
	3C8	RW	Pixel Address Register (write mode)
	3C9	RW	Pixel Data Registers 00 - FF

AVGA2 Extended Registers (summary):

AVGA2 Configuration Register; CF(15:0), written by RESET low, from MD(15:0)

AVGA2 Test Registers; TR0(7:0)-TR7(7:0), written by TWRN low

The following new registers are extensions of the standard VGA registers and are read/write locked by a single Unlock Register in the Sequencer.

Sequencer
SR6: Unlock ALL extensions (xxx1x010 or 12H)
SR7: Extended Sequencer Modes
SR8: EEPROM Control
SR9: Scratch-pad register 0
SRA: Scratch-pad register 1
SRB: VCLK0 numerator value
SRC: VCLK1 numerator value
SRD: VCLK2 numerator value
SRE: VCLK3 numerator value
SRF: DRAM control
SR10: Graphics Cursor X position
SR11: Graphics Cursor Y position
SR12: Graphics Cursor Attributes
SR13: Graphics Cursor Pattern Address Offset
SR1B: VCLK0 denominator & post scaler value
SR1C: VCLK1 denominator & post scaler value
SR1D: VCLK2 denominator & post scaler value
SR1E: VCLK3 denominator & post scaler value

Graphics Controller
GR9: Offset register 0
GRA: Offset register 1
GRB: Graphics Controller mode extensions

CRTC
R19: Interlace End
R1A: Interlace Control
R1B: Extended Display Controls

AVGA2 CONFIGURATION REGISTER, CF15:0

This 16-bit register configures the AVGA2 into various modes of operation. Software cannot access this register. Data present on the Memory Data Bus MD(15:0) is loaded into this register by power-on reset. Data on the MD bus is supplied at reset by internal pull-up resistors (nominally 250K) and optional, external pull-down resistors (nominally 6.8K). A pull-down resistor will cause the corresponding configuration register bit to be a '0' ; therefore, if no pull-down resistors are installed, power-on reset loads this register with data FFFFh

CF15 (MD15) Latched input for optional configuration switch; readable at extended sequencer index 7, bit 7
CF14 (MD14) Latched input for optional configuration switch; readable at extended sequencer index 7, bit 6
CF13 (MD13) Latched input for optional configuration switch; readable at extended sequencer index 7, bit 5
CF12 (MD12) Latched input for optional configuration switch; readable at extended sequencer index 7, bit 4

CF11 (MD11) DRAM Timing Select
0: High performance
1: Default

CF10 (MD10) MCLK frequency select bit 1
CF9 (MD9) MCLK frequency select bit 0
00: 50.11363 MHz
01: 44.74431 MHz
10: 41.16477 MHz
11: 37.58523 MHz

CF8 (MD8) ROM BIOS size
0: 64K @ C0000-CFFFF
1: 32K @ C0000-C7FFF

CF7 (MD7) System Bus Interface
0: Microchannel
1: PC/XT/AT System Bus Interface

CF6 (MD6) 8-bit/16-bit Video BIOS ROM select
0: 16-bit BIOS ROM
1: 8-bit BIOS ROM

CF5 (MD5) VCLK3 source (external source is provided for testing)
0: External oscillator using pin VCLK as input
1: Internal clock generator.

CF4 (MD4) MCLK source;
0: External , MCLK pin is configured as an input
1: Internal, MCLK pin is configured to output the internally generated MCLK

CF3 (MD3) Select VGA Enable Register Address (AT bus interface only))
0: VGA Enable Register is mapped into 46E9.
1: VGA Enable Register is mapped into 46E8.
This bit changes the I/O port address of the VGA Enable Register normally mapped into port 46E8 for use in motherboard implementations of the AVGA2. This bit allows disabling the AVGA2 through port 46E9 instead. Therefore, any VGA Video Adapters, enabled by port 46E8, won't conflict with the AVGA2. The AVGA2 BIOS must be configured for this option. In Microchannel bus configuration, the VGA enable register is 3C3h and this bit has no effect .

CF2 (MD2) Map Out 2K BIOS ROM Addresses
0: Ignore 2K addresses, C6000-C67FF, output pin EROMN remains high for these addresses.
1: Include all 32K addresses, C0000-C7FFF, in the decode for the BIOS ROM.

CF1 (MD1) Enable BIOS ROM Zero Wait
0: Enable output ZERON to be driven active when accessing the BIOS ROM.
1: Output ZERON remains high impedance when accessing the BIOS ROM.

CF0 (MD0) Internal RAMDAC disable
0: External RAMDAC used with DCLK, BLNKn and VD7:0
1: Internal RAMDAC used

AVGA2 Extended Register details - Sequencer

SR2: Map Mask (AVGA2 EXTENSIONS)

	IBM	AVGA2, extended
D7	Reserved=0	Enable writing pixel 7
D6	Reserved=0	Enable writing pixel 6
D5	Reserved=0	Enable writing pixel 5
D4	Reserved=0	Enable writing pixel 4
D3	Map 3 Enable	Enable writing pixel 3
D2	Map 2 Enable	Enable writing pixel 2
D1	Map 1 Enable	Enable writing pixel 1
D0	Map 0 Enable	Enable writing pixel 0

The functions of these bits are changed from the normal VGA Map Mask functions to Pixel Mask functions if AVGA2 extended write modes 4 or 5 are programmed. These bits are also changed to Pixel Mask functions if Write Mode 1 is selected and bit GRB(1)=1. (See GR5 and GRB register descriptions for Extended Write Modes details).

Bits (7:4) of this register are read/write if Graphics Controller Mode Extensions Register bit GRB(2)=1. If GRB(2)=0, then bits (7:4) of this register are read only and 0.

Extended Write Modes 4 and 5 are selected by setting bit GRB(2)=1 and writing 4 or 5 to the Graphics Mode Register (05). There are no defined (non-extended) VGA write modes 4 or 5. The role of this Map Mask register, functioning as a Pixel Mask, is to allow masking any individual pixels within the group of eight being written; clearing bit n to 0 prevents the nth pixel of the group from being written to video memory. (The pixels are numbered, as displayed left to right, from n = 7 to 0, respectively.) Therefore, the Pixel Mask function allows preserving the foreground and background colors of selected pixels.

SR6: Unlock ALL extensions (xxx1x010 or 12H)
This register is loaded with the decode of data bits 4,2,1, & 0. After loading xxx1x010 into this register, to unlock all extensions, this register is readable as 0010010; if loaded with any other value, this register reflects the locked condition, and it is readable as 0Fh.

SR7: Extended Sequencer Modes
D7:4 Reflects the RESET state of switch inputs CF(15:12) and are Read Only.

D3 Select hardware(=0) or software(=1) control of output drivers and IOCHRDY during video memory read cycles. See bits D2 and D1, which enable this bit.

D2 Software control of output drivers and IOCHRDY. This bit has no effect if SR7(3)=0.
0: Enable output drivers and IOCHRDY during video memory read cycles
1: Disable output drivers and IOCHRDY only during memory read cycles; allows shadowed video memory to be read instead.

D1 Enable controlling the output drivers and IOCHRDY. During video memory read cycles, this bit has no effect if Configuration bit CF(5)=0; also see bits D3 & D2.
0: Override; no control of output drivers and IOCHRDY, either by pin VCLK (hardware control) or by SR7(2) (software control).
1: Enable control either by input pin VCLK or by SR7(2).

AVGA2 Extended Register details - Sequencer

SR7: Extended Sequencer Modes (cont.)

D0 Selects High Resolution 256 Color Mode. The video data shift registers are configured so that one character clock equals eight pixels. This bit also enables true packed-pixel memory addressing.

"True packed-pixel addressing" means that all bytes are stored at every consecutive location in video memory; by contrast, in Chain 4 addressing as used in Mode 13h, consecutive pixels are stored in consecutive maps 0 through 3, at every fourth location in video memory.

SR8: EEPROM Control

D7 EEPROM data input, reflects state of EEDI input (read only)

D6 Two cards installed; disables 16-bit video memory access requests through pin MCS16N.

D5 Latch ESYNC and EVIDEO inputs. When this bit is low, the ESYNC and EVIDEO bi-directional pins directly control the BLNKN, VSYNC, HSYNC, and video P(7:0) output drivers. Setting this bit to 1 latches the levels present on the ESYNC and EVIDEO pins. The latched levels, therefore, control the output drivers. This bit is used when accessing the EEPROM, through the ESYNC and EVIDEO pins (see bits D4-D2); it should be set high before setting bit D4 high, and it should be cleared to 0 after clearing bit D4 to 0.

D4 Enable EEPROM data out and SK through bi-directional pins EVIDEO and ESYNC; setting this bit to 1 causes these pins to output bits D3 and D2 of this register.

D3 Data output to the EEPROM, through bi-directional pin EVIDEO, if bit D4 of this register is set to 1.

D2 EEPROM clock (SK), through bi-directional pin ESYNC, if bit D4 of this register is set to 1.

D1 Enable EEPROM data input from EEDI.

D0 EEPROM enable, determines the state of output EECS

Note: The EEPROM is an *option*, that may be used to store video configuration data such as monitor timing options. The EEPROM can replace switches at lower cost and with greater flexibility. Typically the EEPROM will be a 1K bit serial EEPROM compatible with the XL93C46.

SR9: Scratch-pad register 0

D7:0 Eight bit read/write register, reserved for BIOS use.

SRA: Scratch-pad register 1

D7:0 Eight bit read/write register, reserved for BIOS use.

AVGA2 Extended Register details - Sequencer

SRB: VCLK0 numerator value
SR1B: VCLK0 denominator & post scaler value

SRC: VCLK1 numerator value
SR1C: VCLK1 denominator & post scaler value

SRD: VCLK2 numerator value
SR1D: VCLK2 denominator & post scaler value

SRE: VCLK3 numerator value
SR1E: VCLK3 denominator & post scaler value

The 7-bit Numerator (N), 5-bit Denominator (D), and 1-bit Post Scaler (P) for each video clock (VCLK) determines its frequency according to the following expression:

$$VCLKn\ (MHz) = \frac{OSC \times N}{D \times [1 + P]}$$

Where: OSC = input clock, 14.31818 MHz
N = Register Data bits SRi(6:0), i=B,C,D,E
D = Register Data bits SR1i(5:1)
P = Register Data bits SR1i(0)

The registers are read/write and preset with the following data by RESET:

CLOCK	FREQ (MHz)	N	D	P	SRi(6:0)	SR1i(5:0)
VCLK0	25.1802	102	29	1	66h	3Bh
VCLK1	28.3251	91	23	1	5Bh	2Fh
VCLK2	41.1648	69	24	0	45h	30h
VCLK3	36.0818	129	25	1	7Eh	33h
Other tested frequencies:						
	31.193	122	28	1	7Ah	39h
	39.992	81	29	0	51h	3Ah
	44.907	69	22	0	45h	2Ch
	50.113	56	16	0	38h	20h
	64.010	76	17	0	4Ch	22h
	75.169	84	16	0	54h	20h

Video Dot Clock Selection

The dot clock is selected by a combination of Configuration Bit CF(5), Miscellaneous Output Register (I/O port 3C2) bits 3 & 2, and input EDCLK, as shown in the following table:

CF(5)	EDCLK	3C2(3)	3C2(2)	Dot Clock Selected
X	X	0	0	VCLK0
X	X	0	1	VCLK1
X	1	1	0	VCLK2
1	1	1	1	VCLK3
0	1	1	1	VCLK input
X	0	1	X	DCLK input

CF(4)=0 selects external MCLK. If CF(4)=0 and SRF(1:0) are both low and CF(5)=0 then the DOT CLOCK selected is the VCLK input pin. In addition, signals EDCLK and bits 3C2(3:2) have no effect.

AVGA2 Extended Register details - Sequencer

SRF: DRAM control
Note: The Read-only bits of this register are for BIOS use.

D7:4 Reserved

D3 DRAM data width
0 = 8 bit
1 = 16 bit
This bit should be set to 1 if 4 DRAMS are installed. It has one level of buffering; at the end of each horizontal scan line's refresh interval, this bit is sampled and transferred to the active timing logic.

D2 RAS timing as selected by MD11; Read-only
0 = High performance; RAS high=3MCLK, RAS low=4MCLK
1 = Standard; RAS high=2.5 MCLK, RAS low = 3.5MCLK

D1:0 MCLK frequency as selected by MD(10:9); Read-only

D(1)	D(0)	Frequency
0	0	50.11363 MHz
0	1	44.74431 MHz
1	0	41.16477 MHz
1	1	37.58523 MHz

SR10,30,50,70,90,B0,D0,F0 : Graphics Cursor X position
D7:0 Upper 8 bits of the 11-bit cursor X (pixel) position
Index bits D7:5 = Lower 3 bits of the 11-bit cursor X (pixel) position

This 11-bit register defines the offset in pixels from the start of active video (upper left corner) to the horizontal position of the Graphics Cursor. The data written to this register passes through two levels of buffering. Register data is transferred to the first level by writing to the Graphics Cursor Y position register and to the second, final level by each leading edge of Vertical Sync (or odd field sync in interlaced modes).

SR11,31,51,71,91,B1,D1,F1 : Graphics Cursor Y position
D7:0 Upper 8 bits of the 11-bit cursor Y (pixel) position
Index bits D7:5 = Lower 3 bits of the 11-bit cursor Y (pixel) position

This 11-bit register defines the offset in pixels from the start of active video (upper left corner) to the vertical position of the Graphics Cursor. The data written to this register passes through one level of buffering. The graphics cursor Y position is updated at each leading edge of Vertical Sync (or odd field sync in interlaced graphics modes).

NOTE: The graphics cursor position registers use the upper three bits of the sequencer index register as part of the position data. This allows a single sixteen bit I/O write to the sequencer (3C4/3C5) to update the X or Y position. If 11, 31, 51, ... F1 is written to 3C4 without writing to 3C5, then reading 3C4 will reflect the **previously** stored 3 bits of cursor position. Writing to 3C5 will update the entire cursor position.

AVGA2 Extended Register details - Sequencer

SR12: Graphics Cursor Attributes
D7:2 Reserved

D1 Allow access to RAMDAC Cursor colors.
This bit should be set to 1 for programming the hardware graphics cursor color values. The RAMDAC look-up-table extended locations 256 & 257 are accessible as locations 0h (cursor background) & xFh (cursor foreground). This provides for a graphics cursor that is completely independent of the display data colors.

D0 Graphics Cursor Enable

SR13: Graphics Cursor Pattern Address Offset
D7:6 Reserved

D5:0 Selects one of 64 cursor patterns at the top of display memory.

The data written to this register passes through two levels of buffering. Data is transferred from this register to the first level by each leading edge of Vertical Sync (or odd field sync in interlaced graphics modes). Data is transferred to the final level only at the end of each horizontal scan line's refresh interval, in order to protect display memory.

AVGA2 Extended Register details - Graphics Controller

GR0: Set/Reset Register (AVGA2 EXTENSIONS)

	IBM Write modes 0 or 3	AVGA2 Extended Write modes 4 or 5
D7	Reserved=0	Write mode 5 Background color bit 7
D6	Reserved=0	Write mode 5 Background color bit 6
D5	Reserved=0	Write mode 5 Background color bit 5
D4	Reserved=0	Write mode 5 Background color bit 4
D3	Set/Reset Map 3	Write mode 5 Background color bit 3
D2	Set/Reset Map 2	Write mode 5 Background color bit 2
D1	Set/Reset Map 1	Write mode 5 Background color bit 1
D0	Set/Reset Map 0	Write mode 5 Background color bit 0

The functions of these bits are changed from the normal VGA Set/Reset definition to define the Background Color if AVGA2 extended write mode 5 is selected (See GR5 and GRB register descriptions). Bits (7:4) of this register are read/write if Graphics Controller Mode Extensions Register bit GRB(2) is set to 1. If GRB(2)=0, then bits (7:4) of this register are read only and 0. If GRB(2)=1, write modes 0 or 3 use only bits (3:0) of this register, although bits (7:4) are read/write.

GR1: Enable Set/Reset Register (AVGA2 EXTENSIONS)

	IBM Write mode 0	AVGA2 Extended Write modes 4 or 5
D7	Reserved=0	Write modes 4/5 Foreground col bit 7
D6	Reserved=0	Write modes 4/5 Foreground col bit 6
D5	Reserved=0	Write modes 4/5 Foreground col bit 5
D4	Reserved=0	Write modes 4/5 Foreground col bit 4
D3	En Set/Reset Map 3	Write modes 4/5 Foreground col bit 3
D2	En Set/Reset Map 2	Write modes 4/5 Foreground col bit 2
D1	En Set/Reset Map 1	Write modes 4/5 Foreground col bit 1
D0	En Set/Reset Map 0	Write modes 4/5 Foreground col bit 0

The functions of these bits are changed from the normal VGA Enable Set/Reset definition to define the Foreground Color if AVGA2 extended write modes 4 or 5 are selected (See GR5 and GRB register descriptions). Bits (7:4) of this register are read/write if Graphics Controller Mode Extensions Register bit GRB(2) is set to 1. If GRB(2)=0, then bits (7:4) of this register are read only and 0. If GRB(2)=1, write mode 0 uses only bits (3:0) of this register, although bits (7:4) are read/write.

AVGA2 Extended Register details - Graphics Controller

GR5: Mode Register (AVGA2 EXTENSIONS)

D7	Reserved =0	[IBM]
D6	256 color mode (used in standard VGA Mode 13h)	[IBM]
D	Shift Register Mode	[IBM]
D4	Odd/Even	[IBM]
D3	Read Type	[IBM]
D2	Reserved=0, if GRB(2)=0	[IBM]
	or Write Mode bit 2, if GRB(2)=1	[AVGA2]
D(1:0)	Write Mode bits 1 and 0	[IBM]

All bits except D2 control normal VGA functions. Bit D2 is used as a third Write Mode select bit if Graphics Controller Mode Extensions register GRB bit 2 is set to 1. Otherwise, bit D2 is read only and 0, and has no effect. Clearing GRB(2) to 0 directly clears GR5(2) to 0 and keeps it 0.

Setting bit D2 to 1 allows selection of AVGA2 extended write modes 4 and 5; extended write modes 6 and 7 are reserved for future definition. Write modes 0 through 3, the standard VGA write modes, are selectable if bit D2 = 0.

The AVGA2 extended write modes operate on 8-pixels at a time in 256-color graphics modes with packed-pixel addressing. They can be used for text write, line draw, or pattern fills.

Write Mode 4: 256 color text write mode - preserve background
The Graphics Controller Enable Set/Reset Register's (01) 8-bit value is the foreground color selected when CPU data is 1. If CPU data bit is 0 then that pixel is not changed by the write. The Enable Set/Reset Register is normally 4 bits, but is extended to 8 bits by setting GRB(2) to 1. The Sequencer's map mask register, extended to 8 bits, also inhibits writes. Setting GRB(2)=1 also extends the normally 4-bit Sequencer Map Mask Register to 8 bits.

Write Mode 5: 256 color text write mode - foreground/background
Like write mode 4, except that the Graphics Controller Set/Reset Register's (00) 8-bit value is used as the background color to be written to the pixels selected by CPU data=0. The Set/Reset Register is normally 4 bits, but is extended to 8 bits by setting GRB(2) to 1. The Map Mask register in the Sequencer, extended to 8-bits, is used to inhibit writes to selected pixels. Setting GRB(2)=1 also extends the normally 4-bit Sequencer Map Mask Register to 8 bits.

Note: Both these modes should be used with X8 addressing selected.

GR9: Offset register 0

D7 Reserved

D6:0 System address offset for DISPLAY MEMORY A(18:12), added to XA(16:12).
This provides access to the 512K display memory with 4K granularity.
Options: Active for all addresses (GRB_0=0) or Selected when SA15=0 (GRB_0=1)

GRA: Offset register 1

D7 Reserved

D6:0 System address offset for DISPLAY MEMORY A(18:12), added to XA(16:12).
This provides an optional 32K window into the 512K display memory with 4K granularity.
Options: Inactive (GRB_0 0=0) or Selected when SA15=1 (GRB_0=1)

AVGA2 Extended Register details - Graphics Controller

GRB: Graphics Controller Mode Extensions

D7:4 Reserved

D3 Selects the memory read data latches to be eight bytes wide, instead of the normal four bytes.

This bit can be used in Write Mode 1, in order to rewrite 8 latched pixels (64 bits) back into display memory. This bit should be used in X8 addressing mode only. Write Mode 1 is selected by writing 01 to the Graphics Mode Register (05).

If this bit is low, and X8 Addressing is not selected, then Write Mode 1 rewrites 4 latched pixels back into display memory, as the normal VGA operation.

D2 Enable AVGA2 extended write modes. Setting this bit to 1:
(1) Enables up to 8 bytes to be transferred to display memory for every CPU byte cycle.
(2) Enables bit GR5(2) to enable selecting extendedWrite Modes 4 and 5;
(3) Extends GR0(3:0) to GR0(7:0);
(4) Extends GR1(3:0) to GR1(7:0);
(5) Extends SR2(3:0) to SR2(7:0).

D1 X8 Addressing for 256-color mode block moves and extended write modes.

D0 Enable Offset Register 1

This bit, when set to 1, allows System Address input SA15, when 1, to select Offset Register 1 as the Offset used in generating memory addresses XMA(18:12); otherwise, Offset Register 0 is selected to generate the memory addresses.

The XMA(18:12) addresses are the sum of XA(16:12) and an Offset Register. The Offset Register is either Offset Register 0 (Register GR9) or Offset Register 1 (Register GRA). Addresses XA(14:12) always equal the System Address inputs SA(14:12). Address XA(16) equals System Address input SA16 only if the AVGA2 is mapped into video memory segments A000 and B000 [GR6(3:2)=00]; otherwise, XA(16) is 0. Address XA(15) equals System Address input SA15 if the AVGA2 is mapped either into A000 and B000 [GR6(3:2)=00] or into A000 only [GR6(3:2)=01], and if Register bit GRB(0) is 0; otherwise, address XA(15) is 0.

The AVGA2 adds addresses XA(16:12) to the Offset Register OFF(6:0) to generate XMA(18:12), as follows:

0	0	XA(16)	XA(15)	XA(14)	XA(13)	XA(12)
+OFF(6)	OFF(5)	OFF(4)	OFF(3)	OFF(2)	OFF(1)	OFF(0)
XMA(18)	XMA(17)	XMA(16)	XMA(15)	XMA(14)	XMA(13)	XMA(12)

AVGA2 Extended Register details - CRTC

R19: Interlace End
D7:0 Ending Horz. character count for odd field VSYNC.

R1A: Interlace Control
D(7:2) Reserved

D1 Enable double-buffered Display Start Address loading for animation effect:
The display start will be updated on the VSYNC following a write to Start Address Low only, writes to Start Address High will be double-buffered.

D0 Enable interlaced sync and video data in graphics mode, or interlaced sync only in text mode.
Setting this bit to 1 also affects the output pin IRQ (Interrupt Request), if bit R1B(3)=0. An interrupt is generated by the trailing edge of Vertical Display Enable (end of the active scan) only at the end of an odd field; therefore, the interrupt may be used to signal the processor that one frame has been completed. Normally, if this bit is cleared to 0, the interrupt is generated by the trailing edge of Vertical Display Enable during every, non-interlaced frame.

R1B: Extended Display Controls
D7 Reserved

D6 Select Page Mode Alpha (132 column text)
This bit should be set to 1 for 132-column text modes. This mode uses fast-page CAS cycles to DRAM to get text font data. This allows for text modes with VCLKs higher than 30Mhz, but does not support the standard VGA dual font feature.

D5 Internal DAC Power-Down
Setting this bit to 1 powers down the internal DAC. If Configuration Register bit CF(0)=0 (External DAC installed), then this bit has no effect.

D4 DCLK Frequency Divider Control
Setting this bit to 1 affects the output pin DCLK (DAC Clock). The frequency of this clock output is constrained to equal the frequency selected by Miscellaneous Output Register bits 3C2(3:2). The frequency of this clock is unaffected by programming Attribute Controller Register bit 3C0.10(6) or Sequencer Register bit SR1(3), which normally can select a divide-by-two dot clock to appear at this output pin. This bit is provided for support of some plasma flat-panels.

D3 Select Blink Counter Interrupt
Setting this bit to 1 affects the output pin IRQ (Interrupt Request). An interrupt is generated by the trailing edge of Vertical Display Enable (end of the active scan) if the CRT Controller's character blink/cursor blink counter has reached its last count (1Fh); therefore, the interrupt may be used to signal the processor, primarily in board test applications, that during the next frame the cursor and any blinking characters will be blinked on. The character blink rate is every 32 VSYNCs and the cursor blink rate is every 16 VSYNCs. In interlaced modes the blink counter is clocked only on the odd fields.

AVGA2 Extended Register details - CRTC

R1B: Extended Display Controls (cont.)

D2 Extended Cursor (High) Location address bit 16 (used with 4 DRAMs)

D1 0=IBM address wrap for 64K memory maps (IBM compatibility with 512K memory)
1=Extended address wrap for 128K maps with 512K memory (allows 4 pages of Mode 13)

This bit controls the following functions:

(1) If this bit is set to 1 and Chain 4 addressing [SR4(3)=1] is selected, then DRAM addresses A0 and A1, normally supplied by CPU Addresses XMA(14) and XMA(15), are instead supplied by addresses XMA(16) and XMA(17). The XMA(18:12) addresses are the sum of XA(16:12) and an Offset Register. Refer to the description of Register bit GRB(0) for definitions of XMA(18:12) and XA(16:12).

(2) If this bit is set to 1 and CRT Controller Double Word Addressing [R14(6)=1] is selected, then DRAM addresses A0 and A1, normally supplied by CRTC Character Counter Addresses CA(12) and CA(13), are instead supplied by addresses CA(14) and CA(15). This provides 4 displayable pages in Mode 13h. With 4 DRAMs installed, Character Counter Address CA(16) is added, allowing an 128Kb displayable page.

(3) If this bit is cleared to 0, the CRT Controller's Character Address Counter is 16 bits wide, compatible with IBM's. Even with 4 DRAMs installed, the Counter does not access the 2nd 256Kb. If this bit is set to 1, the Counter is 17 bits.

D0 Extended display start address bit 16 (used with 4 DRAMs only)

AVGA2 Extended Register details - Miscellaneous

Input Status 1 [port 3?A] (AVGA2 EXTENSION)

	IBM & AVGA2 Non-Interlaced Modes	AVGA2 Interlaced Modes Only
D7	Reserved=0	Reserved=0
D6	Reserved=0	Odd Field=0; Even Field=1
D5	Diagnostic 0	Diagnostic 0
D4	Diagnostic 1	Diagnostic 1
D3	Vertical Retrace	Vertical Retrace
D2	Reserved=1	Reserved=1
D1	Reserved=0	Reserved=0
D0	Display Enable	Display Enable

As shown in the table above, bit D6 of Input Status Port 1 indicates the field number of an interlaced frame, if interlaced mode is programmed by setting CRTC Register R1A(0)=1. (Refer to the section, "1024x768 INTERLACED GRAPHICS").

132-Column Alphanumeric Mode

This extended video mode is selected if R19 bit D6 (in CRTC) is set to a 1. The Video Dot Clock should be 41.164 MHz, selected by programming Miscellaneous Output Register bit 3=1 and bit 2=0. The Sequencer is programmed for 8-dot character intervals, with a non-divided dot clock.

The Character Map(s) should be loaded while this mode is selected, because the memory organization of the Character Maps differs from the normal VGA case. Loading the Character Maps, however, needs no special address translation incorporated into programming, because the AVGA2 remaps Video memory automatically when this mode is selected. The Character Maps should be loaded by unchained (sequential) addressing, the AVGA2 having been mapped into System Address segment A0000 for 64Kb locations, with the Sequencer Map Mask Register programmed to enable writing to Plane 2. Subsequently, the AVGA2 should be programmed for Chain 2 addressing, with Planes 0 & 1 enabled, as is normally the case in an Alphanumeric mode.

This mode does not support displaying two different character maps on the screen at the same time, as determined by character attribute bit 3 in the normal VGA operation. However, one of eight Character Maps can be selected for the entire screen display, by programming the Sequencer Character Map Select Register (3C5, index 03) bits 2:0 with a Character Map number. The Character Map number represents one 8Kb segment of the total available 64Kb of Character Maps in this mode. Each Character Map number corresponds to an 8Kb offset from the initial System Address segment where the Maps are loaded initially: Map 0 is loaded into A0000-A1FFF, Map 1 into A2000-A3FFF, etc. Note the functional change of the Character Map Select register bits 2:0 when this mode is selected; the remaining bits 5:3 are not used.

The AVGA2 uses both Plane 2 and Plane 3 physical DRAM pages for Character Map storage in this mode, although the Character Maps appear to be loaded into Plane 2 only. The AVGA2 remaps character generator dot patterns of all lower 128 character codes into Plane 2, and all the upper 128 into Plane 3. Only half of each 64Kb physical Plane is therefore used, providing a total of eight, 8Kb Character Maps.

The following CRT Controller parameters are recommended in this mode:

Data	Register
9FH	Horizontal Total (index 0)
83H	Horiz Display Enable End (index 1)
84H	Start Horizontal Blanking (index 2)
82H	End Horizontal Blanking (index 3)
8AH	Start Horizontal Retrace (index 4)
9EH	End Horizontal Retrace (index 5)
42H	Offset (index 13H)

Other AVGA2 Features

Video memory data FIFO depth is eight levels for all graphics and text modes with 2 DRAM. With 4 DRAM the FIFO depth is four levels for all text and eight levels for all graphics modes.

The write buffer is two levels deep for 2 DRAM and four levels deep for 4 DRAM.

If the Color Don't Care register (GR7) is set to 00, and if Read Mode 1 is selected (GR5(3)=1), then a CPU memory read cycle will still load the internal data latches, but will not have wait-states added. This is useful for both 16-color and 256-color block moves where the CPU is using Write Mode 1 to move data with the data latches and never actually reads any screen data. Write buffer is effectively only one level deep.

Hardware Cursor

The hardware cursor is used in 16-color planar and 256-color packed-pixel modes to provide a pointer for graphical user interfaces. A hardware cursor (mouse pointer) will improve performance because the screen data will not have to be rewritten when the cursor is moved, and it will improve the appearance of the screen by providing a smoothly moving cursor. The cursor is a 32x32 pixel array of two planes:

Cursor Plane 0 = invert plane
Cursor Plane 1 = opaque plane

Each pixel of the cursor 'floats' over a corresponding pixel of the screen. The opaque Cursor Plane controls the selection of VGA video data or cursor data. A '1' in the opaque Cursor Plane selects cursor data. The cursor is one of two colors; for an external RAMDAC, the cursor data is either 00 or FF for P7:0, and for the internal RAMDAC the cursor color is supplied by two extra LUT locations for cursor colors 0 & xFh. The invert Cursor Plane controls the selected video data. VGA video data (7:0) is inverted (both to P7:0 and to the internal RAMDAC) if the invert bit is 1 and the opaque bit is 0. The video data is inverted after the effect of any other VGA registers. The invert bit controls the cursor color (0 or 1) if the opaque bit is a 1. The cursor therefore has four possible states for each pixel:

00 = Transparent
01 = Inverted VGA video data
10 = Cursor Color 0
11 = Cursor Color 1

The cursor position is defined relative to the upper left corner of the active display screen (border is not included), and sets the upper left corner of the 32x32 cursor. The cursor location X is in pixels and Y is in scan lines. The cursor position on the screen is changed only on the VSYNC following a write to the Y location register (SEQ index 11h). The location 0,0 is the first pixel of the top active video scan line.

The cursor data is located in the upper 16K of display memory at all times (upper 4K in each memory map). There are 64 possible cursor patterns that are selected by the cursor pattern offset register (SEQ index 13h). Each cursor pattern is 256 bytes; 64 bytes in each logical memory map. The first 32 bytes of each memory map are Cursor Plane 0, the last 32 bytes are Cursor Plane 1. One byte from each memory map forms the Cursor Plane for each scan line. Map 0 data is displayed first, with bit D7 being the first pixel. The CPU can write cursor data either in unchained mode or in chain-four mode with true packed- pixel addressing.

In packed-pixel addressing, with CH4 addressing selected, the cursor data write is all of Cursor Plane 0 first, followed by Cursor Plane 1. For example: if SR13h=00 (cursor pattern address offset), then the first byte of the first scan line of the Cursor Plane 0 is located at address 1F000h in MAP0 (for 512K).

The Cursor CRT Controller data read replaces the DRAM refresh on the active cursor display lines. The cursor data read is two CAS page reads; one for Cursor Plane 0 and one for Cursor Plane 1. All four display memory maps are read. The 17-bit (for 512K of memory) CRT Controller address is generated as follows:

HCR(17:14) = all 1's
HCR(13:8) = cursor pattern offset register SR13(5:0)
HCR(7) = cursor plane read select
HCR(6:2) = cursor scan line counter 4:0

1024x768 Interlaced Graphics

All video timing is specified for AVGA2 outputs P(7:0), BLNKN, VSYNC, and HSYNC. To obtain video timing at R,G,B outputs, add 3 dot clock delays through the DAC, from P(7:0) to R,G,B.

Vertical sync (VSYNC) transitions coincide with negative transitions of Horizontal Sync (HSYNC) at the end of the odd field. The position of the negative edge of HSYNC is determined by CRTC register 05 (Horizontal Retrace End). At the end of the even field, however, transitions of VSYNC coincide with negative transitions of an additional, internal H/2 sync pulse. The position of the internal H/2 sync negative edge is determined by extended CRTC register 19h (Interlace End). The value to be programmed into register 19h depends upon the values chosen for CRTC registers 04 and 05.

Even-numbered scan lines (numbered from 0) are displayed in the even field. Odd-numbered scan lines (numbered from 1) are displayed in the odd field. Scan line 0 is above scan line 1 on the display screen. Whether the field is odd or even can be determined by reading bit 6 of Input Status Port 1 (3?A). If 3?A(6)=0, then the field is odd.

If Vertical Interrupt is enabled (CRTC Register 3?5.10h) and interlaced mode is selected (3?5.1A(0)=1), then an interrupt is generated by the trailing edge of Vertical Display Enable (end of the active scan) only at the end of an odd field; therefore, the interrupt may be used to signal the processor that one frame has been completed. In normal, non-interlaced VGA operation (3?5.1A(0)=0), the interrupt is generated by the trailing edge of Vertical Display Enable during every, non-interlaced frame.

Neither border nor line compare is supported

Dot Clock	44.74431 MHz (22.3492 ns)
Total VCLKS per line:	1264
Total horizontal character count per line	1264/8 = 158 = 9Eh
CRTC REG 00h Horizontal Total = (9Eh-5)	99h
Maximum displayed pixels per line	1024
Total horizontal character count per line:	1024/8 = 128 = 80h
CRTC REG 01h Horizontal Display End = (80h-1)	7Fh
Horizontal front porch in VCLKS	13

Horizontal front porch in this mode (no border) is the interval between the end of 1024th displayed pixel (at the P(7:0) video outputs of the AVGA2) and the start of HSYNC (the HSYNC output of the AVGA2)

In normal VGA timing, the video outputs P(7:0) are delayed in graphics mode, relative to horizontal sync timing, by 2 characters and 5 dot clocks. This means, for example, that if the horizontal retrace start register (00) is programmed with the same value as the horizontal display enable end register (01), then horizontal display enable will go inactive (i.e., the right boundary of the last displayed pixel) 21 dot clocks after HSYNC starts.

In 8514A-compatible timing, the relative delay of the video outputs to horizontal sync is 2 characters and 3 dot clocks, totalling 19 dot clocks. The AVGA2 implements this delay by adding a delay of 2 dot clocks to the HSYNC delay path if interlaced timing is selected (R1A(0)=1). Because Vertical Sync Timing is aligned on HSYNC boundaries, VSYNC is also delayed by 2 dot clocks, relative to normal VGA timing.

1024x768 Interlaced Graphics

Horizontal Sync width in VCLKS (Positive polarity)	176
Horizontal back porch in VCLKS	51
Vertical period (field rate, lines)	408.5
Frame rate (Lines)	817

The frame consists of alternating even and odd fields. The number of lines per frame, N, must be odd; if m is programmed into the Vertical Total registers, then N=2m+5. The Vertical timing counter maximum count is m during the odd field, and m+1 during the even. There are m+2 lines in the odd field, and m+3 in the even.

m = (N-5)/2 = 406 =	196h
==> CRTC REG 06h Vert Total =	96h
==> CRTC REG 07h(0) Vert Total bit 8 =	1
==> CRTC REG 07h(5) Vert Total bit 9 =	0

VERTICAL DISPLAYED LINES PER FIELD	384
VERTICAL DISPLAYED LINES PER FRAME	768
==> CRTC Vert Display = (384-1)=	17Fh
==> CRTC REG 12h Vert Display =	7Fh
==> CRTC REG 07h(1) Vert Display bit 8 =	1
==> CRTC REG 07h(6) Vert Display bit 9 =	0

VERTICAL SYNC WIDTH (LINES)	4

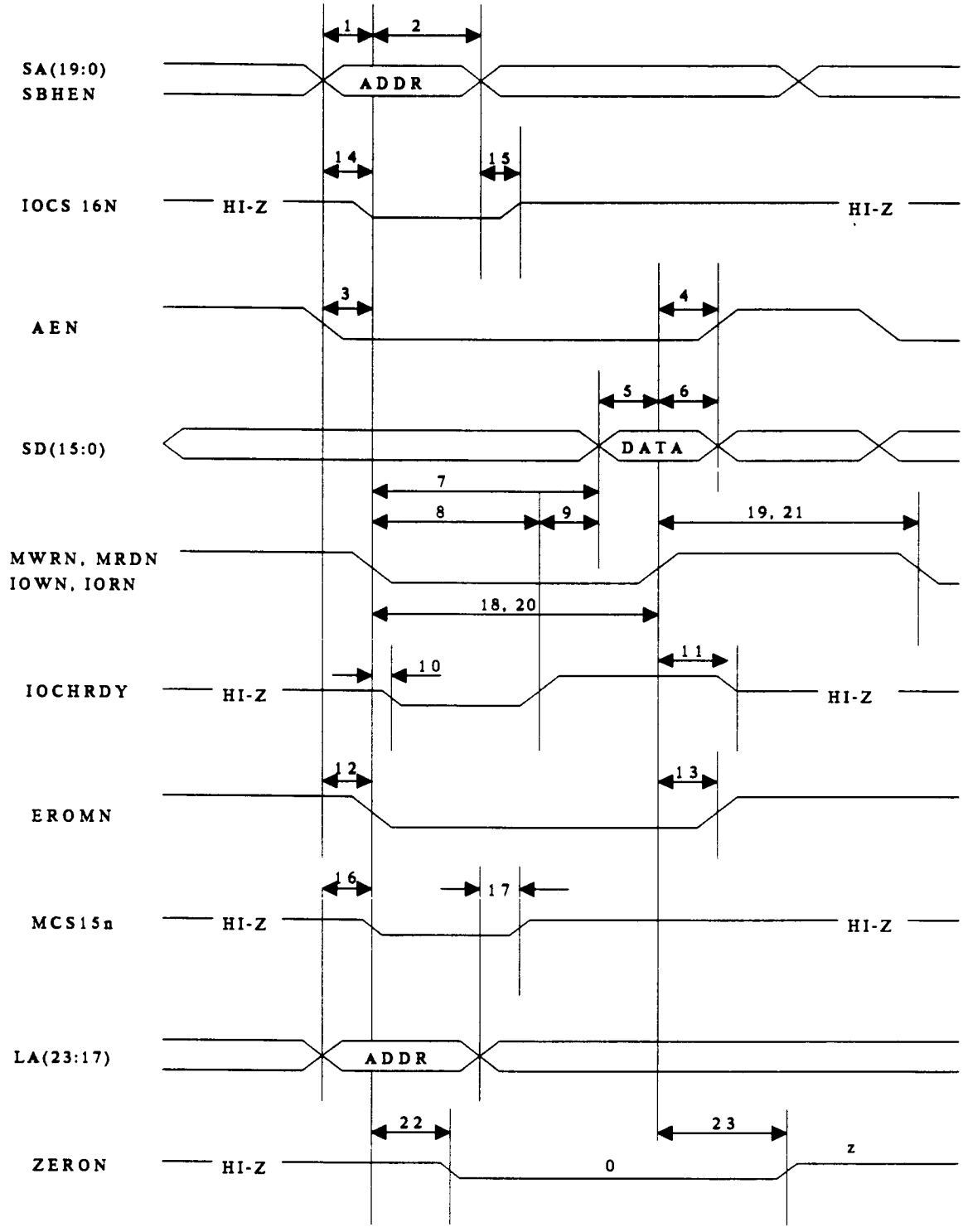
Vertical front porch (lines), Start of EVEN field Odd field end to vertical sync rising edge.	0.0
Vertical front porch (lines), Start of ODD field Even field end to vertical sync rising edge.	0.5
Vertical back porch (lines), Start of EVEN field Vertical sync falling edge to even field start.	20.0
Vertical back porch (lines), Start of ODD field Vertical sync falling edge to odd field start.	20.5

Vertical sync has positive polarity. Vertical sync position is programmed with a value specific for the end of the odd field; vertical sync position is delayed relative to this position, by 1/2 horizontal period at the end of the even field.

==> CRTC REG 10h Vert Ret Start=	7Fh
==> CRTC REG 07h(2) Vert Ret Start bit 8 =	1
==> CRTC REG 07h(7) Vert Ret Start bit 9 =	0
==> CRTC REG 11h Vert Ret End (bits 3:0) =	83h

A.C. TIMING CHARACTERISTICS AT Mode Bus Interface		
Parameter	**Minimum**	**Maximum**
1a. sa(19:0) setup to mrdn, mwrn low	20ns	---
1b. sa(19:0) setup to iorn, iown low	15ns	---
1c. sbhen setup to mrdn, mwrn, iorn, iown	5ns	---
2a. sa(19:0) hold from to mrdn, mwrn low	15ns	---
2b. sa(19:0) hold from iorn, iown low	18ns	---
2c. sbhen hold from mrdn, mwrn, iorn, iown	5ns	---
3. aen setup to iorn/iown low	16ns	---
4. aen hold from iorn/iown high	5ns	---
5. sd(15:0) write data setup to iown high	5ns	---
6a. sd(15:0) read data hold from iorn high	---	28ns
6b. sd(15:0) read data hold from mrdn high	---	20ns
6c. sd(15:0) write data hold from iown high	15ns	---
6d. sd(15:0) write data hold after mwrn high	10ns	---
7a. sd(15:0) read data valid from iorn low	---	60ns (240pf load)
7b. sd(15:0) write data valid after mwrn low		3t
8. iochrdy high from mwrn/mrdn low	8.7ns	
9. Memory read data valid from iochrdy high	---	15ns (240pf load)
10. iochrdy low from mwrn/mrdn low	9ns	39ns (240pf load)
11. iochrdy tristate from mwrn/mrdn high	4ns	12ns (240pf load)
12. eromn low from valid a(23:15)	---	42ns (20pf load)
13. eromn hold from mrdn high	---	20ns (20pf load)
14. sa(19:0) valid to iocs16 low	---	60ns (240pf load)
15. iocs16 hold from sa(19:0)	---	23ns (240pf load)
16. La(23:17) valid to memcs16 low	---	70ns (240pf load)
17. memcs16 hold from La(23:17)	---	17ns (240pf load)
18. iown low	90ns	
19. iown high	80ns	
20. mwrn low	3t	
21. mwrn high	3t	
22a. mrdn low to zeron low (BIOS rom access)	5.6ns	21.6ns
22b. mrdn low to zeron low (vid. mem access)	6t + 20ns	100t
22c. mwrn low to zeron low (iochrdy high)	5.7ns	21.8ns
23a. mrdn high to zeron tristate (BIOS rom access)	4.5ns	17.6ns
23b. mrdn high to zeron tristate (vid. mem access)	5.0ns	19ns

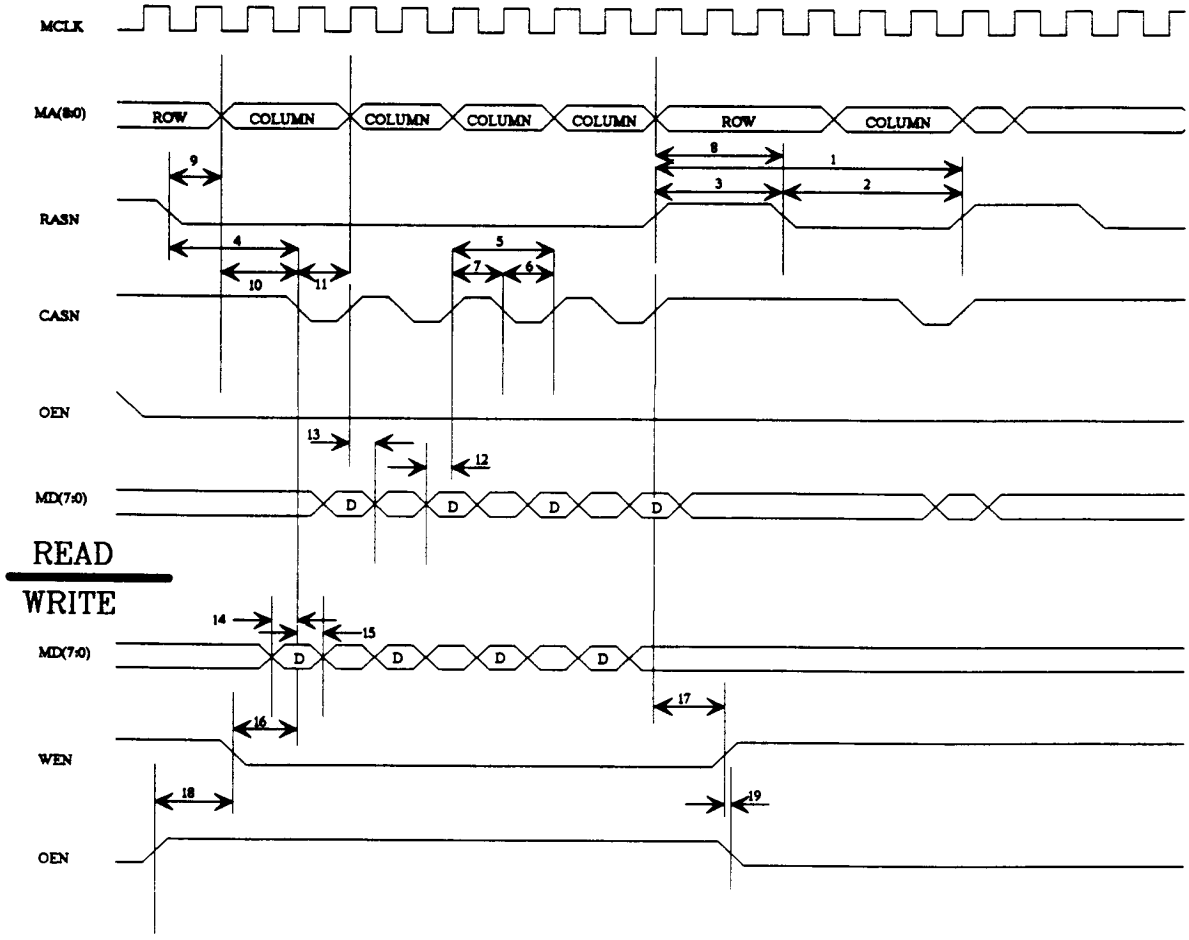
Note: t = MCLK period



AT MODE BUS INTERFACE TIMING

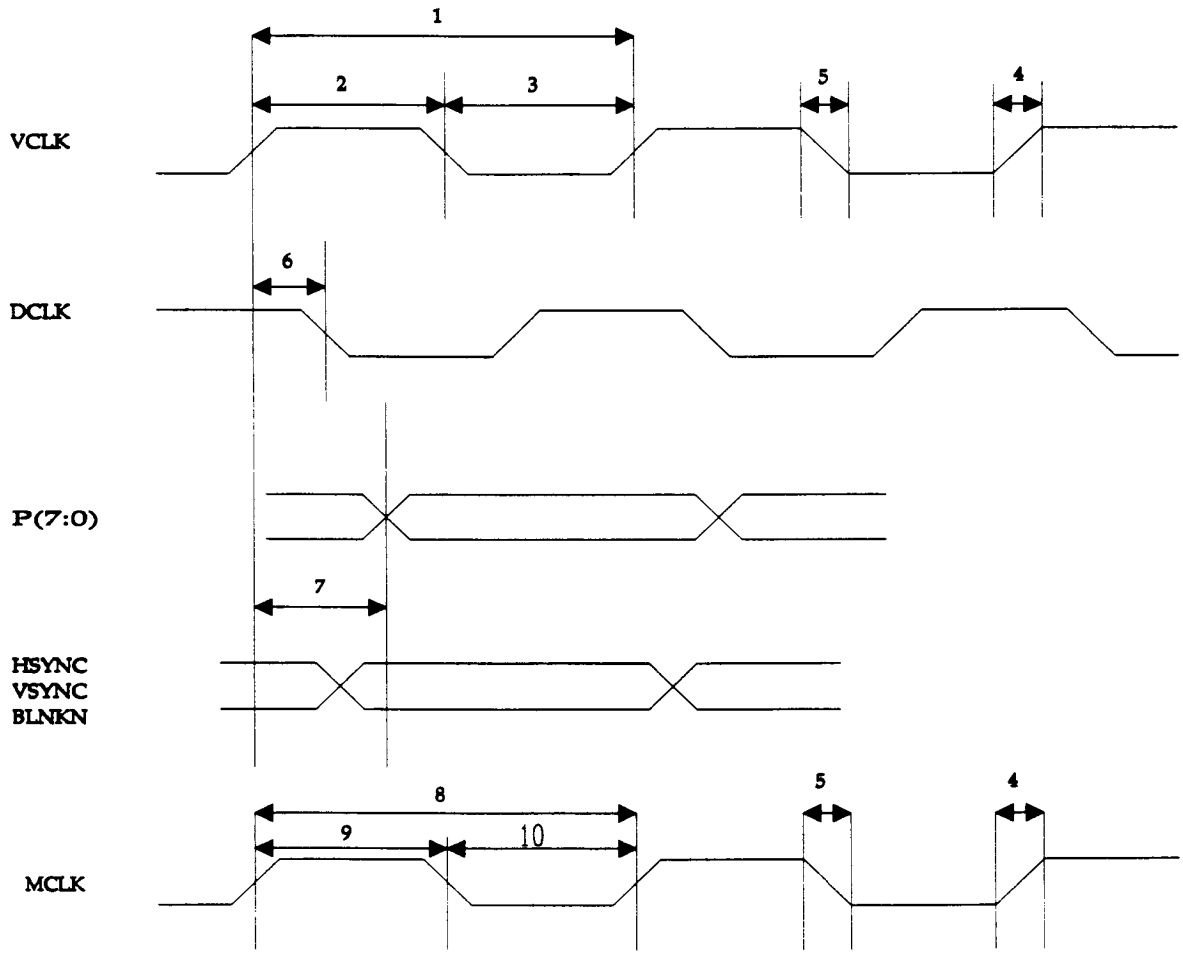
DRAM Timing		
Parameter	**Minimum**	**Maximum**
1. RASN cycle time - standard DRAM	6t	6t
2. RASN pulse width low - standard DRAM	3.5t - 13.2ns	
3. RASN high time (precharge) - standard DRAM	2.5t + 4ns	
4. RASN low to CASN low - standard DRAM	2.5t - 8.4ns	2.5t - 2.9ns
1*. RASN cycle time - high performance DRAM	7t	7t
2*. RASN pulse width low - high perf. DRAM	4t - 13.2ns	
3*. RASN high time (precharge) - high perf. DRAM	3t + 4ns	
4*. RASN low to CASN low - high perf. DRAM	3t - 8.4ns	3t - 2.9ns
5. CASN cycle time	2t	2t
6. CASN pulse width low	1t	1t
7. CASN high time (precharge)	1t	1t
8. Row address setup to RASN low	1.5t	1.5t
9. Row address hold time to RASN low	1t	1t
10. Column address setup to CASN low	1t	1.5t - 8.9ns
11. Column address hold to CASN low	1t + 1ns	1t + 6.2ns
12. Read Data valid before CASN high	0ns	---
13. Read Data hold after CASN high	10ns	---
14. Write Data setup to CASN low	1t	2t
15. Write Data hold after CASN low	1t	1t
16. WE0N, WE1N low setup CASN low	2t	2t
17. WE0N, WE1N low hold after CASN high	1t	1t
18. OEN high before WE0N low	1t	1t
19. OEN low after WE0N high	1ns	4ns

Note: All outputs have 20pf loading


MCLK
MA(8:0)
ROW
COLUMN
COLUMN
COLUMN
COLUMN
ROW
COLUMN
RASN
CASN
OEN
MD(7:0)
D
READ
WRITE
MD(7:0)
WEN
OEN
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19

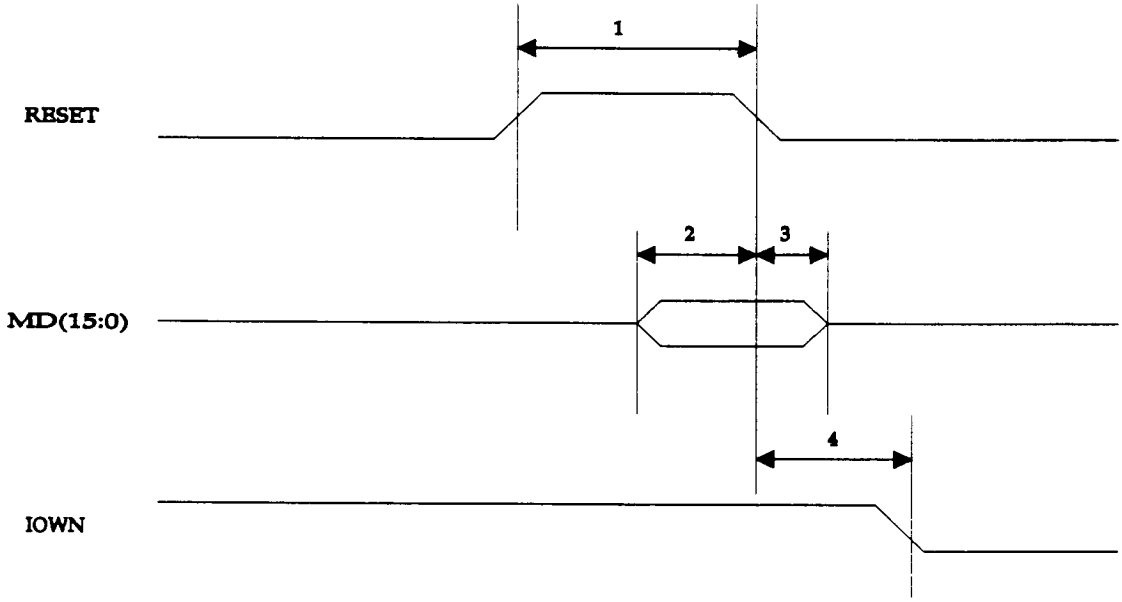
DRAM TIMING

Clock Timing		
Parameter	**Minimum**	**Maximum**
1. VCLK period	13.3ns	---
2. VCLK high	40%	---
3. VCLK low	40%	---
4. Clock Rise time	---	3ns
5. Clock Fall time	---	3ns
6. VCLK to DCLK delay	9.3ns	36ns (50pf load)
7a. VCLK to Hsync, Vsync or Blnkn delay	9.8ns	36ns (150pf load)
7b. VCLK to P(7:0) delay	8.5ns	37ns (50pf load)
8. MCLK period	20ns	---
9. MCLK High	9ns	---
10. MCLK Low	9ns	---



Reset Timing		
Parameter	**Minimum**	**Maximum**
1. minimum reset width	12t	---
2. set-up time between md and reset	10ns	---
3. hold time between md and reset	20ns	---
4. Reset low to first iown	12t	---

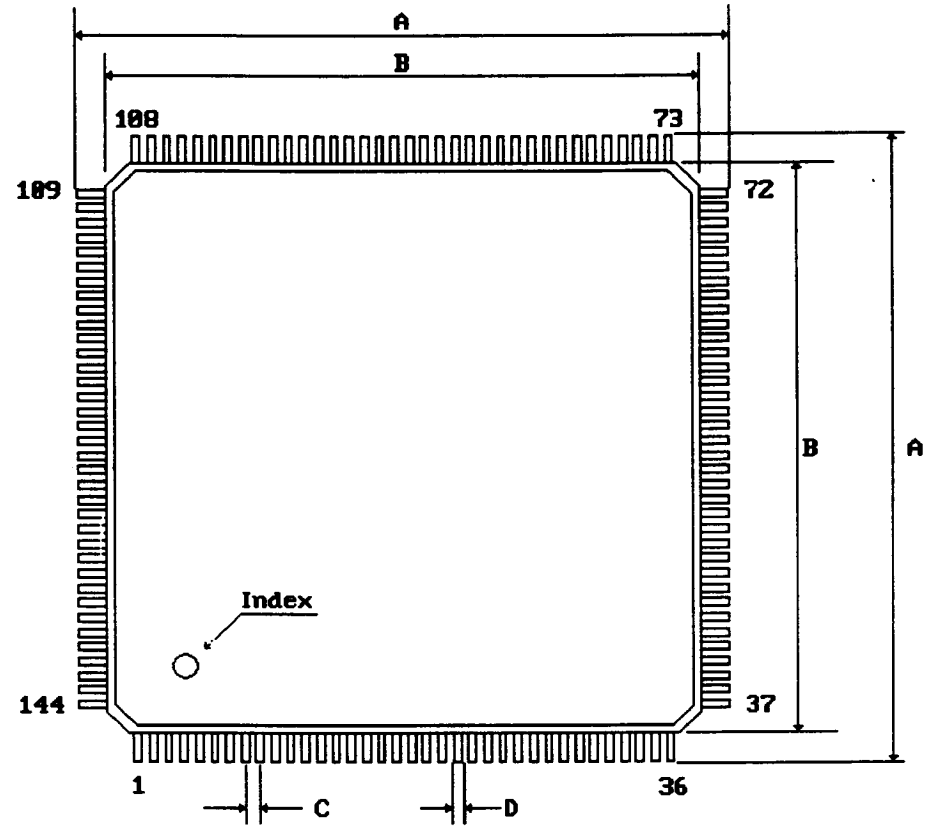
Note: t = MCLK period

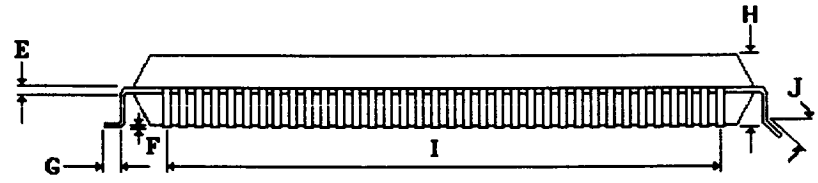


ABSOLUTE MAXIMUM RATINGS	
Supply voltage, VDD	7V
Voltage, from any pin to VSS	-0.5 to +7V
Operating free-air temperature range	0° C to 70° C
Storage temperature range	-65° C to 150° C
Power Dissipation	1.5 Watt

D.C. CHARACTERISTICS (0 to 70 C)					
Symb	**Parameter**	**Min**	**Nom**	**Max**	**Unit**
Vdd	Supply voltage	4.75	5.00	5.25	V
Idd	Supply current		230	300	mA
Vih	High-level input voltage	2.0		Vdd + 0.5	V
Vil	Low-level input voltage	-0.5		0.8	V
Voh	High-level output voltage	2.4		Vdd	V
Vol	Low-level output voltage	Vss		0.4	V
Iih	High-level input current (Vil=Vdd)			10	uA
Iil	Low-level input current (Vdd=5.25V; Vil=-0.5V)		-0.05	mA	
Ioh,	High-level output current			See pin descriptions	
Iol	Low-level output current				
Ioz	Output Leakage Current (Voh=VDD; Vol=VSS)			+ 10	uA
Vref	DAC Output Level Comparator	320	337	354	mV

PACKAGE OUTLINE - 144 PIN POFP (PLASTIC QUAD FLAT PACK)





SYMBOL	mm.	SYMBOL	mm.
A	31.47 + 0.69	F	0.23 + 0.13
B	28.00 + 0.10	G	0.69 + 0.25
C	0.65 + 0.10	H	3.40 + 0.15
D	0.30 + 0.10	I	22.75 + 0.10
E	0.15 + 0.05	J	0^{o} - 12^{o}

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The Company

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† U.S. Patent No. 4,293,783

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