GLINT R5®

Reference Guide Volume IV -
Physical Characteristics

PROPRIETARY AND CONFIDENTIAL INFORMATION

3D*labs*®

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Issue 4

Proprietary Notice

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Change History

Document	Issue	Date	Change
172.1.4	1	15/02/2000	Creation
172.1.4	2	25/07/2000	Update thermal chap 10 to R5, start final update all pins to R5, 150600; complete, 120700; corrected Thermal and Electrical data, 210700;
172.1.4	3	15/09/2000	First full release post engineering review.
172.1.4	4	05/03/2001	Added operating range in chap. 11, bug reports and software fixes from chip bringup, new R5 package photo, interleave mode note, minor format changes.

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Package Diagrams

The R5 package is a thermally-enhanced PBGA (TEPBGA) 529 ball custom design.

Figure 7-1 Package Diagram (Top View)

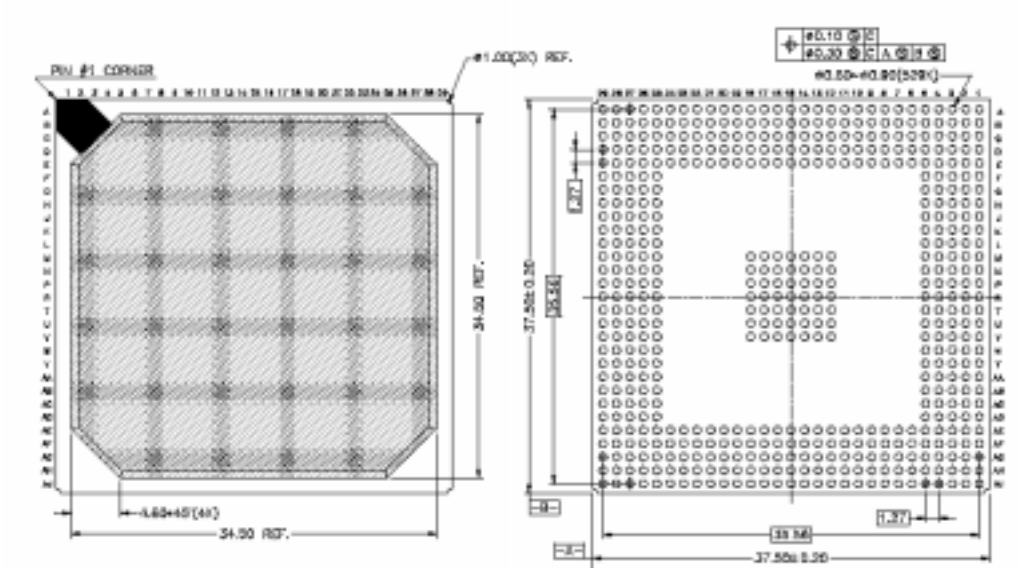

Figure 7-2 Package Diagram (Top and Bottom Views)

Table 7-1 Package dimensions

Body Size	37.5 x 37.5 mm
Body Height	2.38 mm
Substrate thickness	0.61 mm
Ball pitch	1.27 mm
Ball pad opening	0.6 mm

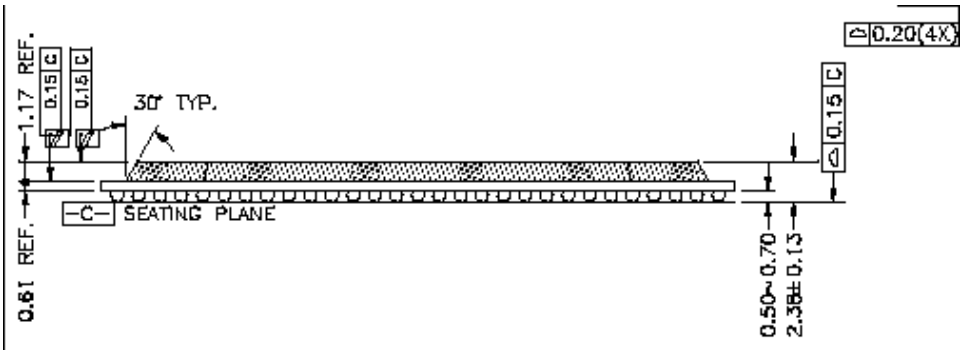

Figure 7-3 Package Diagram (Section View)

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Pin Assignment

8.1 Pinlist by Number

The table below provides a brief description of each pin. It is organized alphabetically by pin number.

The pin type definitions used are:

I/O: Input Signal (tolerates 2.5 and 3.3 VDC PCI and AGP4X standards)

GND: Ground

VSS_3.3: Power at 3.3V

VSS_2.5: Power at 2.5 Volts

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	A 1	NC(1)		
POWER	A 2	NC(2)		
POWER	A 3	VCCS25_1_0	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	A 4	MDATB(18)	BIDIR	Memory B Data at 320MHz
POWER	A 5	GND01	POWER	Core and IO ground supply = 0v
MEM	A 6	SSTLVREF(1)	POWER	SSTL Class 1 I/O reference voltage = VCCS25_2 = 1.25v
POWER	A 7	VCCT33_2_2	POWER	TTL I/O Driver supply (VCC)=3.3v
MEM	A 8	SSTLVP(3)	POWER	SSTL Class 1 pre-driverIO supply = 2.5v
POWER	A 9	GND(59)	POWER	Core and IO ground supply = 0v
MEM	A10	MDATB(2)	BIDIR	Memory B Data at 320MHz
VIDEO	A11	DFPINTERRUPT	IN	General purpose interrupt
VIDEO	A12	VIDEOMERGEHSYNCN	BIDIR	Horizontal strobe used in multichip configs (tie off if unused)
VIDEO	A13	VIDEOMERGEDATA2	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A14	VIDEOMERGEDATA7	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A15	VIDEOMERGEDATA9	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A16	VIDEOMERGEDATA18	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	A17	VIDEOMERGEDATA 20	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A18	VIDEOMERGEDATA 24	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A19	VIDEOMERGEDATA 31	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A20	VIDEOMERGEDATA 36	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	A21	GND(6)	POWER	Core and IO ground supply = 0v
VIDEO	A22	VIDEOMERGEDATA 43	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	A23	VCCT33_2_1	POWER	TTL I/O Driver supply (VCC)=3.3v
VIDEO	A24	VIDEOMERGEDATA 54	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	A25	GND(4)	POWER	Core and IO ground supply = 0v
VIDEO	A26	VIDEOMERGEDATA 58	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	A27	VCCT33_2_0	POWER	TTL I/O Driver supply (VCC)=3.3v
POWER	A28	NC(5)	N/C	
POWER	A29	NC(6)	N/C	
POWER	AA 1	GND(65)	POWER	Core and IO ground supply = 0v
VIDEO	AA 2	DACSFADJ	BIDIR	DAC full scale adjust - connect via 226 ohm resistor to ground.
VIDEO	AA 3	DACAG(3)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AA 4	PLLAG_1	POWER	PLL analogue ground = 0v (isolated from GND)
VIDEO	AA 5	DACAG(2)	POWER	DAC analogue ground = 0v (isolated from GND)
MEM	AA25	MDATA(17)	BIDIR	Memory A Data at 320MHz
MEM	AA26	MDATA(20)	BIDIR	Memory A Data at 320MHz
MEM	AA27	MDATA(19)	BIDIR	Memory A Data at 320MHz
MEM	AA28	MDATA(18)	BIDIR	Memory A Data at 320MHz
POWER	AA29	GND(2)	POWER	Core and IO ground supply = 0v
VIDEO	AB 1	VIDBLUE	BIDIR	Analogue blue component
VIDEO	AB 2	DACVAA_1	POWER	DAC analogue power = 3.3v
VIDEO	AB 3	DACCOMP	POWER	See DAC spec for details
VIDEO	AB 4	DACVAA_2	POWER	DAC analogue power = 3.3v
VIDEO	AB 5	DACVREF	BIDIR	See DAC spec for details
MEM	AB25	MDATA(15)	BIDIR	Memory A Data at 320MHz
MEM	AB26	MDMA(2)	BIDIR	Memory A Data Write Masks at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	AB27	SSTLVREF(3)	POWER	SSTL Class 1 I/O reference voltage = VCCS25_2 = 1.25v
MEM	AB28	MDQA(2)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	AB29	MDATA(16)	BIDIR	Memory A Data at 320MHz
VIDEO	AC 1	VIDGREEN	BIDIR	Analogue green component
VIDEO	AC 2	DACAG(1)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AC 3	DACVAA(0)	POWER	DAC analogue power = 3.3v
POWER	AC 4	VCCS25_1_1	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	AC 5	VDD15	POWER	Core logic power = 1.8v
POWER	AC25	VDD5	POWER	Core logic power = 1.8v
MEM	AC26	MDATA(16)	BIDIR	Memory A Data at 320MHz
MEM	AC27	MDATA(16)	BIDIR	Memory A Data at 320MHz
MEM	AC28	MDATA(16)	BIDIR	Memory A Data at 320MHz
POWER	AC29	VCCS25_3_2	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	AD 1	VIDRED	BIDIR	Analogue green component
AGP	AD 2	TESTMODE	IN	Production test global enable (Active high)
VIDEO	AD 3	DACAG(0)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AD 4	VIDVSYNC	BIDIR	DAC Vertical sync/config bit
POWER	AD 5	VDD16	POWER	Core logic power = 1.8v
POWER	AD25	VDD6	POWER	Core logic power = 1.8v
MEM	AD26	MDATA(11)	BIDIR	Memory A Data at 320MHz
MEM	AD27	MDATA(10)	BIDIR	Memory A Data at 320MHz
MEM	AD28	MDATA(9)	BIDIR	Memory A Data at 320MHz
MEM	AD29	MDATA(8)	BIDIR	Memory A Data at 320MHz
POWER	AE 1	GND66	POWER	Core and IO ground supply = 0v
VIDEO	AE 2	TCLKIN	BIDIR	External T clock Input
VIDEO	AE 3	VCLKIN	BIDIR	Production test V clock Input
VIDEO	AE 4	VIDHSYNC	OUT	DAC Horizontal sync
POWER	AE 5	VDD17	POWER	Core logic power = 1.8v
POWER	AE 6	VDD18	POWER	Core logic power = 1.8v
POWER	AE 7	VDD19	POWER	Core logic power = 1.8v
AGP	AE 8	PCIRSTN	IN	RST# Reset (3.3v)
AGP	AE 9	DMASIDEBAND(0)	IN	Private sideband port (Tie high if unused)
AGP	AE10	PCIGNTN	IN	Gnt# Grant (3.3v)
AGP	AE11	AGPRBFN	BIDIR	RGF# Read buffer full (AGP only) (3.3v)
AGP	AE12	AGPSBSTBN	OUT	SB_STB# Sideband strobe (agp only) differential strobe used in agp4x only (1.5v).

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AE13	AGPSBA(4)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AE14	PCIAD(31)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE15	PCIAD(26)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE16	PCIAD(21)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE17	PCIIDSEL	IN	
AGP	AE18	PCIAD(20)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE19	PCIFRAMEN	BIDIR	Frame# Cycle Frame(3.3v)
AGP	AE20	PCIAD(14)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE21	PCIAD(10)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE22	AGPADSTB(0)	IN	AD_STB0 (agp only)
POWER	AE23	VDD7	POWER	Core logic power = 1.8v
POWER	AE24	VDD8	POWER	Core logic power = 1.8v
POWER	AE25	VDD9	POWER	Core logic power = 1.8v
MEM	AE26	MDMA(1)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	AE27	SSTLVP(7)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	AE28	MDQA(1)	BIDIR	Memory A 160MHz bi-directional strobe
POWER	AE29	GND3	POWER	Core and IO ground supply = 0v
VIDEO	AF 1	MCLKIN	BIDIR	External M clock input
VIDEO	AF 2	KCLKIN	BIDIR	External K clock input
VIDEO	AF 3	SCLKIN	BIDIR	External M clock input
VIDEO	AF 4	VIDEOEXTCTRL	BIDIR	Input only as config
VIDEO	AF 5	VIDDDCCLK	BIDIR	
VIDEO	AF 6	ROMWEN	OUT	ROM write enable (active low)
VIDEO	AF 7	SBDATA	BIDIR	
AGP	AF 8	PCICLK	IN	Clk PciClk (3.3v)
AGP	AF 9	PCIINTAN	OUT	INTA# Interrupt A open drain
AGP	AF10	AGPST(0)	BIDIR	ST Status bus (agp only) (1.5-3.3v)
AGP	AF11	AGPSBA(2)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AF12	AGPSBA(0)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AF13	AGPSBA(5)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AF14	PCIAD(28)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF15	PCIAD(29)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF16	AGPADSTB(1)	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AGP	AF17	PCIAD(19)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF18	AGPV3(1)	BIDIR	AGP I/O Reference voltage = VCCA 15/2(1.67v or 0.75v)

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AF19	PCIIRDYN	BIDIR	IRDY# Initiator ready (3.3v)
AGP	AF20	PCIPAR	BIDIR	PAR Parity (3.3v)
AGP	AF21	PCIAD(13)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF22	PCIAD(8)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF23	PCIAD(7)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF24	PCIAD(5)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF25	AGPVREF	BIDIR	AGP I/O Reference voltage = VCCA 15/2 (1.67v or 0.75v)
MEM	AF26	MDATA(3)	BIDIR	Memory A Data at 320MHz
MEM	AF27	MDATA(5)	BIDIR	Memory A Data at 320MHz
MEM	AF28	MDATA(6)	BIDIR	Memory A Data at 320MHz
MEM	AF29	MDATA(7)	BIDIR	Memory A Data at 320MHz
POWER	AG 1	VCCS25_1_	POWER	SSTL IO driver supply (VCC) = 2.5v
POWER	AG 2	NC[9]	N/C	No-connect pins
POWER	AG 3	NC[11]	N/C	No-connect pins
AGP	AG 4	TEXTUREDOWNLOADINT	OUT	Texture download interrupt.
VIDEO	AG 5	PLLDISABLE	IN	Disable PLL's
VIDEO	AG 6	ROMSELECTN	OUT	ROM Select(active low)
VIDEO	AG 7	VIDRIGHTEYE	BIDIR	Right eye signal for stereo/config bit
AGP	AG 8	PCIFIFOINDIS	BIDIR	Private sideband port(input in test/config only)-leave open if unused
AGP	AG 9	DMASIDEBAND[1]	IN	Private sideband port(tie high if unused)
AGP	AG10	PCIREQN	OUT	REQ# Request[3.3v]
AGP	AG11	AGPST[2]	BIDIR	ST Status bus (agp only) [3.3V]
AGP	AG12	AGPSBA[1]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AG13	AGPSBA[6]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AG14	PCIAD(27)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG15	PCIAD(25)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG16	AGPADSTBN[1]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGP	AG17	PCIAD(17)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG18	PCIAD(16)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG19	PCITRDYN	BIDIR	TRDY# Target Ready[3.3v]
AGP	AG20	PCIAD(15)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG21	PCIAD(12)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG22	PCICBEN[0]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AG23	AGPADSTBN[0]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGP	AG24	PCIAD(4)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG25	PCIAD(0)	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
MEM	AG26	MDATA(1)	BIDIR	Memory A Data at 320MHz
MEM	AG27	MDATA(2)	BIDIR	Memory A Data at 320MHz
MEM	AG28	MDATA(4)	BIDIR	Memory A Data at 320MHz
POWER	AG29	VCCS25_3_3	POWER	SSTL IO driver supply (VCC) = 2.5v
VIDEO	AH 1	PLLVAA_	POWER	PLL analogue power = 3.3v
POWER	AH 2	NC(10)	N/C	No-connect pins
VIDEO	AH 3	RENDERSYNCN	BIDIR	Rasterizer resync for multichip solutions(core)
AGP	AH 4	TESTSELECT[0]	IN	Production test mode select
AGP	AH 5	TESTSELECT[2]	IN	Production test mode select
VIDEO	AH 6	ROMOEN	OUT	ROM Output Enable(active low)
VIDEO	AH 7	SBCLK	BIDIR	
AGP	AH 8	PCIFIFOOUTDIS	BIDIR	Private sideband port(input in testconfig only)-leave open if unused
AGP	AH 9	DMASIDEBAND[1]	IN	Private sideband port(tie high if unused)
AGP	AH10	AGPPIPEN	OUT	PIPE#-Pipelined request(agp only)[3.3V]
AGP	AH11	AGPV3[x]	POWER	AGP pre-driver IO supply =3.3v
AGP	AH12	AGPSBSTB	OUT	SB_STB Sideband strobe (agp only)-(differential in AGP4x)[1.5V-3.3V]
AGP	AH13	AGPSBA[7]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AH14	PCIAD(30)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH15	PCIAD(24)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH16	PCIAD(23)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH17	PCIAD(22)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH18	PCICBEN[2]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AGP	AH19	PCIDEVSELN	BIDIR	DEVSEL# Device select[1.5V-3.3V]
AGP	AH20	PCISTOPN	BIDIR	STOP# [3.3v]
AGP	AH21	PCIAD(11)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH22	AGPV3[0]	POWER	AGP pre-driver IO supply =3.3v
AGP	AH23	PCIAD(6)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH24	PCIAD(3)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH25	PCIAD(1)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
MEM	AH26	MDQA[0]	BIDIR	Memory A 160MHz bir-directional strobe
MEM	AH27	MDATA[0]	BIDIR	Memory A data at 320MHz
POWER	AH28	NC[13]	N/C	No-connect pins

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	AH29	NC[14]	N/C	No-connect pins
VIDEO	AJ 1	PLLAG_0	POWER	PLL analogue ground = 0v (islolated from GND)
POWER	AJ 2	NC[12]	N/C	No-connect pins
POWER	AJ 3	VCCT33_0_	POWER	TTL IO driver supply (VCC) = 3.3v
AGP	AJ 4	TESTSELECT[1]	IN	Production test mode select
POWER	AJ 5	GND62	POWER	Core and IO ground supply = 0v
VIDEO	AJ 6	VIDDDCDATA	BIDIR	
POWER	AJ 7	VCCT33_0_	POWER	TTL IO driver supply (VCC) = 3.3v
AGP	AJ 8	PCICLKSEL	IN	Clock select-used to set config capabilities bit
POWER	AJ 9	GND60	POWER	Core and IO ground supply = 0v
AGP	AJ10	AGPST[1]	BIDIR	ST Status bus(agp only)[3.3V]
POWER	AJ11	VCCA15_4_3	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
AGP	AJ12	AGPSBA[3]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
POWER	AJ13	GND51	POWER	Core and IO ground supply = 0v
AGP	AJ14	AGPV3[2]	POWER	AGP pre-driver IO supply =3.3v
POWER	AJ15	VCCA15_4_2	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
AGP	AJ16	PCICBEN[3]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
POWER	AJ17	GND29	POWER	Core and IO ground supply = 0v
AGP	AJ18	PCIAD[18]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
POWER	AJ19	VCCA15_4_1	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
AGP	AJ20	PCICBEN[1]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
POWER	AJ21	GND7	POWER	Core and IO ground supply = 0v
AGP	AJ22	PCIAD[9]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
POWER	AJ23	VCCA15_4_0	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
AGP	AJ24	PCIAD[2]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
POWER	AJ25	GND5	POWER	Core and IO ground supply = 0v
AGP	AJ26	AGPZSET	IN	Analog reference impedance(resistor)-connect to VDDQ via 37.5 ohms
MEM	AJ27	MDMA[0]	BIDIR	Memory A Data write masks at 320MHz
POWER	AJ28	NC[15]	N/C	No-connect pins
POWER	AJ29	NC[16]	N/C	No-connect pins
POWER	B 1	NC[3]	N/C	

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	B 2	NC[4]	N/C	
MEM	B 3	MDATB(21)	BIDIR	Memory B Data at 320MHz
MEM	B 4	MDATB(19)	BIDIR	Memory B Data at 320MHz
MEM	B 5	MDATB(17)	BIDIR	Memory B Data at 320MHz
MEM	B 6	MDQB(2)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	B 7	MDATB(13)	BIDIR	Memory B Data at 320MHz
MEM	B 8	MDATB(9)	BIDIR	Memory B Data at 320MHz
MEM	B 9	MDATB(7)	BIDIR	Memory B Data at 320MHz
MEM	B10	MDATB(0)	BIDIR	Memory B Data at 320MHz
VIDEO	B11	VIDEOMERGEBLANK	BIDIR	DFPBlank or Merge blank input only for config
VIDEO	B12	VIDEOMERGESTROBEIN(2)	IN	Used for multichip solutions - tie unused low.
VIDEO	B13	VIDEOMERGEDATA0	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B14	VIDEOMERGEDATA5	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B15	VIDEOMERGEDATA10	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B16	VIDEOMERGEDATA14	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B17	VIDEOMERGEDATA19	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B18	VIDEOMERGEDATA25	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B19	VIDEOMERGEDATA30	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B20	VIDEOMERGEDATA34	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B21	VIDEOMERGEDATA41	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B22	VIDEOMERGEDATA46	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B23	VIDEOMERGEDATA50	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B24	VIDEOMERGEDATA53	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B25	VIDEOMERGEDATA57	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B26	VIDEOMERGEDATA59	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	B27	VIDEOMERGEDATA61	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	B28	NC[7]	N/C	
POWER	B29	NC[8]	N/C	
POWER	C1	VCCS25_1_2	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	C2	MDQB(3)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	C3	MDATB(23)	BIDIR	Memory B Data at 320MHz
MEM	C4	MDATB(20)	BIDIR	Memory B Data at 320MHz
MEM	C5	MDATB(16)	BIDIR	Memory B Data at 320MHz
MEM	C6	MDATB(15)	BIDIR	Memory B Data at 320MHz
MEM	C7	MDATB(11)	BIDIR	Memory B Data at 320MHz
MEM	C8	MDATB(8)	BIDIR	Memory B Data at 320MHz
MEM	C9	MDATB(6)	BIDIR	Memory B Data at 320MHz
MEM	C10	MDATB(3)	BIDIR	Memory B Data at 320MHz
MEM	C11	MDQB(0)	BIDIR	Memory B 160MHz bi-directional strobe
VIDEO	C12	VIDEOMERGESTROBEIN(1)	IN	Used for multichip solutions - tie unused low.
VIDEO	C13	VIDEOMERGECLOCK	BIDIR	Used for locking PLLs in multi-chip configurations - tie off if unused
VIDEO	C14	VIDEOMERGEDATA6	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C15	VIDEOMERGEDATA11	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C16	VIDEOMERGEDATA15	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C17	VIDEOMERGEDATA23	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C18	VIDEOMERGEDATA27	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C19	VIDEOMERGEDATA32	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C20	VIDEOMERGEDATA37	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C21	VIDEOMERGEDATA40	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C22	VIDEOMERGEDATA45	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C23	VIDEOMERGEDATA48	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C24	VIDEOMERGEDATA52	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	C25	VIDEOMERGEDATA 56	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C26	VIDEOMERGEDATA 60	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C27	VIDEOMERGEDATA 63	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
MEM	C28	MDATA(63)	BIDIR	Memory A data at 320MHz
POWER	C29	VCCS25_3_0	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	D 1	MDATB(24)	BIDIR	Memory B data at 320MHz
MEM	D 2	MDMB(3)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 3	SSTLVP(2)	BIDIR	SSTL Class 1 Pre-driver IO supply =2.5v
MEM	D 4	MDATB(22)	BIDIR	Memory B data at 320MHz
MEM	D 5	MDMB(2)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 6	MDATB(14)	BIDIR	Memory B data at 320MHz
MEM	D 7	MDATB(12)	BIDIR	Memory B data at 320MHz
MEM	D 8	MDMB(1)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 9	MDATB(5)	BIDIR	Memory B data at 320MHz
MEM	D10	MDATB(1)	BIDIR	Memory B data at 320MHz
VIDEO	D11	VIDEOMERGEDATA STROBEOUT	OUT	Strobe for merge data and dFP
VIDEO	D12	VIDEOMERGESTRO BEIN(0)	IN	Used for multi-chip solutions - tie unused low
VIDEO	D13	VIDEOMERGEDATA 48	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D14	VIDEOMERGEDATA 52	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D15	VIDEOMERGEDATA 56	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D16	VIDEOMERGEDATA 60	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D17	VIDEOMERGEDATA 22	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D18	VIDEOMERGEDATA 28	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D19	VIDEOMERGEDATA 29	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D20	VIDEOMERGEDATA 35	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D21	VIDEOMERGEDATA 39	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	D22	VIDEOMERGEDATA 44	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D23	VIDEOMERGEDATA 49	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D24	VIDEOMERGEDATA 51	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D25	VIDEOMERGEDATA 55	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D26	VIDEOMERGEDATA 62	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
MEM	D27	MDATA(60)	BIDIR	Memory A Data at 320MHz
MEM	D28	MDATA(61)	BIDIR	Memory A Data at 320MHz
MEM	D29	MDATA(62)	BIDIR	Memory A Data at 320MHz
POWER	E 1	GND(63)	POWER	Core and IO ground supply = 0v
MEM	E 2	MDATB(25)	BIDIR	Memory B Data at 320MHz
MEM	E 3	MDATB(26)	BIDIR	Memory B Data at 320MHz
MEM	E 4	MDATB(27)	BIDIR	Memory B Data at 320MHz
POWER	E 5	VDD10	POWER	Core logic power = 1.8v
POWER	E 6	VDD11	POWER	Core logic power = 1.8v
POWER	E 7	VDD12	POWER	Core logic power = 1.8v
MEM	E 8	MDATB(10)	BIDIR	Memory B Data at 320MHz
MEM	E 9	MDQB(1)	BIDIR	Memory B 160MHz bidirectional strobe
MEM	E10	MDATB(4)	BIDIR	Memory B Data at 320MHz
VIDEO	E11	MDMB(0)	BIDIR	Memory B data writemasks at 320MHz
VIDEO	E12	VIDEOMERGEVSYNCN	BIDIR	Vertical strobe used I multiple chip configs. Tie off if unused.
VIDEO	E13	VIDEOMERGEDATA 3	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E14	VIDEOMERGEDATA 4	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E15	VIDEOMERGEDATA 12	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E16	VIDEOMERGEDATA 16	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E17	VIDEOMERGEDATA 21	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E18	VIDEOMERGEDATA 26	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E19	VIDEOMERGEDATA 33	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	E20	VIDEOMERGEDATA 38	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E21	VIDEOMERGEDATA 42	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E22	VIDEOMERGEDATA 47	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
POWER	E23	VDD0	POWER	Core logic power = 1.8v
POWER	E24	VDD1	POWER	Core logic power = 1.8v
POWER	E25	VDD2	POWER	Core logic power = 1.8v
MEM	E26	MDATA(57)	BIDIR	Memory A Data at 320MHz
MEM	E27	MDATA(58)	BIDIR	Memory A Data at 320MHz
MEM	E28	MDATA(59)	BIDIR	Memory A Data at 320MHz
POWER	E29	GND0	POWER	Core and IO ground supply = 0v
MEM	F 1	MDATB(28)	BIDIR	Memory B Data at 320MHz
MEM	F 2	MDATA(29)	BIDIR	Memory A Data at 320MHz
MEM	F 3	MDATB(30)	BIDIR	Memory B Data at 320MHz
MEM	F 4	MDATB(31)	BIDIR	Memory B Data at 320MHz
POWER	F 5	VDD13	POWER	Core logic power = 1.8v
POWER	F25	VDD3	POWER	Core logic power = 1.8v
MEM	F26	MDATA(55)	BIDIR	Memory A Data at 320MHz
MEM	F27	MDQA(7)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	F28	MDMA(7)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	F29	MDATA(56)	BIDIR	Memory A Data at 320MHz
POWER	G 1	VCCS25_1_3	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	G 2	MBAB(1)	BIDIR	Memory B Bank address signal
MEM	G 3	MCKEB	BIDIR	Memory B Control signal
MEM	G 4	MBAB(0)	BIDIR	Memory B Bank address signal
POWER	G 5	VDD14	POWER	Core logic power = 1.8v
POWER	G25	VDD4	POWER	Core logic power = 1.8v
MEM	G26	MDATA(53)	BIDIR	Memory A Data at 320MHz
MEM	G27	MDATA(52)	BIDIR	Memory A Data at 320MHz
MEM	G28	MDATA(54)	BIDIR	Memory A Data at 320MHz
POWER	G29	VCCS25_1_3	POWER	SSTL I/O Driver supply (VCC)=2.5v
MEM	H 1	MCKLBN	BIDIR	Memory B 160MHz inverted clock out
MEM	H 2	MRASB	BIDIR	Memory B Control Signal
MEM	H 3	MCASB	BIDIR	Memory B Control Signal
MEM	H 4	MDSFB	BIDIR	Memory B Control Signal
MEM	H 5	MWEB	BIDIR	Memory B Control Signal
MEM	H25	MDATA(51)	BIDIR	Memory A Data at 320MHz
MEM	H26	MDATA(48)	BIDIR	Memory A Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	H27	MDATA(49)	BIDIR	Memory A Data at 320MHz
MEM	H28	MDATA(50)	BIDIR	Memory A Data at 320MHz
MEM	H29	MDMA(6)	BIDIR	Memory A Data Write Masks at 320MHz
POWER	J 1	GND64	POWER	Core and IO ground supply = 0v
MEM	J 2	MADDRB(11)	BIDIR	Memory B Address signal
MEM	J 3	MADDRB(10)	BIDIR	Memory B Address signal
MEM	J 4	MADDRB(9)	BIDIR	Memory B Address signal
MEM	J 5	MCKLB	BIDIR	Memory B 160MHz inverted clock out
MEM	J25	SSTLVP(4)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	J26	MDATA(47)	BIDIR	Memory A Data at 320MHz
MEM	J27	MDQA(6)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	J28	SSTLVREF(2)	POWER	SSTL Class 1 IO reference voltage = VCCS25/2 = 1.25v
POWER	J29	GND1	POWER	Core and IO ground supply = 0v
MEM	K 1	MADDRB(6)	BIDIR	Memory B Address signal
MEM	K 2	MADDRB(4)	BIDIR	Memory B Address signal
MEM	K 3	MADDRB(7)	BIDIR	Memory B Address signal
MEM	K 4	MADDRB(5)	BIDIR	Memory B Address signal
MEM	K 5	MADDRB(8)	BIDIR	Memory B Address signal
MEM	K25	MDATA(46)	BIDIR	Memory A Data at 320MHz
MEM	K26	MDATA(43)	BIDIR	Memory A Data at 320MHz
MEM	K27	MDATA(45)	BIDIR	Memory A Data at 320MHz
MEM	K28	MDATA(42)	BIDIR	Memory A Data at 320MHz
MEM	K29	MDATA(44)	BIDIR	Memory A Data at 320MHz
MEM	L 1	MADDRB(1)	BIDIR	Memory B Address signal
MEM	L 2	MADDRB(0)	BIDIR	Memory B Address signal
MEM	L 3	MADDRB(2)	BIDIR	Memory B Address signal
MEM	L 4	MDQB(4)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	L 5	MADDRB(3)	BIDIR	Memory B Address signal
MEM	L25	MDATA(41)	BIDIR	Memory A Data at 320MHz
MEM	L26	MDATA(39)	BIDIR	Memory A Data at 320MHz
MEM	L27	MDATA(40)	BIDIR	Memory A Data at 320MHz
MEM	L28	MDQA(5)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	L29	MDMA(5)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	M 1	MDATB(34)	BIDIR	Memory B Data at 320MHz
MEM	M 2	MDATB(35)	BIDIR	Memory B Data at 320MHz
MEM	M 3	MDMB(4)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	M 4	SSTLVP(1)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	M 5	MDATB(32)	BIDIR	Memory B Data at 320MHz
MEM	M25	MDATA(35)	BIDIR	Memory A Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	M26	MDATA(38)	BIDIR	Memory A Data at 320MHz
MEM	M27	MDATA(37)	BIDIR	Memory A Data at 320MHz
MEM	M28	MDATA(36)	BIDIR	Memory A Data at 320MHz
MEM	M29	MDATA(34)	BIDIR	Memory A Data at 320MHz
MEM	N 1	MDATB(38)	BIDIR	Memory B Data at 320MHz
MEM	N 2	MDATB(39)	BIDIR	Memory B Data at 320MHz
MEM	N 3	MDATB(35)	BIDIR	Memory B Data at 320MHz
MEM	N 4	MDATB(36)	BIDIR	Memory B Data at 320MHz
MEM	N 5	MDATB(37)	BIDIR	Memory B Data at 320MHz
MEM	N25	MDQA(4)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	N26	MDMA(4)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	N27	MDATA(33)	BIDIR	Memory A Data at 320MHz
MEM	N28	MDATA(32)	BIDIR	Memory A Data at 320MHz
MEM	N29	SSTLVP(5)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	P 1	MDQB(5)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	P 2	MDATB(42)	BIDIR	Memory B Data at 320MHz
MEM	P 3	MDATB(41)	BIDIR	Memory B Data at 320MHz
MEM	P 4	MDMB(5)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	P 5	MDATB(40)	BIDIR	Memory B Data at 320MHz
MEM	P25	MADDRA(0)	BIDIR	Memory A Address signal
MEM	P26	MADDRA(4)	BIDIR	Memory A Address signal
MEM	P27	MADDRA(2)	BIDIR	Memory A Address signal
MEM	P28	MADDRA(1)	BIDIR	Memory A Address signal
MEM	P29	MADDRA(3)	BIDIR	Memory A Address signal
MEM	R 1	MDATB(47)	BIDIR	Memory B Data at 320MHz
MEM	R 2	MDATB(46)	BIDIR	Memory B Data at 320MHz
MEM	R 3	MDATB(45)	BIDIR	Memory B Data at 320MHz
MEM	R 4	MDATB(43)	BIDIR	Memory B Data at 320MHz
MEM	R 5	MDATB(44)	BIDIR	Memory B Data at 320MHz
MEM	R25	MDDRA(8)	BIDIR	Memory A Address signal
MEM	R26	MDDRA(7)	BIDIR	Memory A Address signal
MEM	R26	MDDRA(9)	BIDIR	Memory A Address signal
MEM	R28	MDDRA(6)	BIDIR	Memory A Address signal
MEM	R29	MDDRA(5)	BIDIR	Memory A Address signal
MEM	T 1	SSTLVREF(0)	POWER	SSTL Class 1 IO reference voltage = VCCS25/2 = 1.25v
MEM	T 2	MDMB(6)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	T 3	SSTLVP(0)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	T 4	MDQB(6)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	T 5	MDATB(48)	BIDIR	Memory B Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	T25	MCLKA	BIDIR	Memory A 160MHz Clock out
MEM	T26	MCLKAN	BIDIR	Memory A 160MHz Inverted Clock out
MEM	T27	MDDRA(11)	BIDIR	Memory A Address signal
MEM	T28	MDDRA(10)	BIDIR	Memory A Address signal
MEM	T29	MDSFA	BIDIR	Memory A Control Signal
MEM	U 1	MDATB(50)	BIDIR	Memory B Data at 320MHz
MEM	U 2	MDATB(52)	BIDIR	Memory B Data at 320MHz
MEM	U 3	MDATB(53)	BIDIR	Memory B Data at 320MHz
MEM	U 4	MDATB(51)	BIDIR	Memory B Data at 320MHz
MEM	U 5	MDATB(49)	BIDIR	Memory B Data at 320MHz
MEM	U25	MWEA	BIDIR	Memory A Control signal
MEM	U26	MCKEA	BIDIR	Memory A Control signal
MEM	U27	MBAA(0)	BIDIR	Memory A Bank Address signal
MEM	U28	MCASA	BIDIR	Memory A Control signal
MEM	U29	MRASA	BIDIR	Memory A Control signal
MEM	V 1	MDATB(54)	BIDIR	Memory B Data at 320MHz
MEM	V 2	MDQB(7)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	V 3	MDMB(7)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	V 4	MDATB(56)	BIDIR	Memory B Data at 320MHz
MEM	V 5	MDATB(55)	BIDIR	Memory B Data at 320MHz
MEM	V25	MDATA(30)	BIDIR	Memory A Data at 320MHz
MEM	V26	MDATA(28)	BIDIR	Memory A Data at 320MHz
MEM	V27	MDATA(29)	BIDIR	Memory A Data at 320MHz
MEM	V28	MDATA(31)	BIDIR	Memory A Data at 320MHz
MEM	V29	MBAA(1)	BIDIR	Memory A Bank Address signal
VIDEO	W 1	XTAL(2)	BIDIR	External Crystal connection
MEM	W 2	MDATB(58)	BIDIR	Memory B Data at 320MHz
MEM	W 3	MDATB(60)	BIDIR	Memory B Data at 320MHz
MEM	W 4	MDATB(57)	BIDIR	Memory B Data at 320MHz
MEM	W 5	MDATB(61)	BIDIR	Memory B Data at 320MHz
MEM	W25	MDMA(3)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	W26	MDATA(27)	BIDIR	Memory A Data at 320MHz
MEM	W27	MDATA(24)	BIDIR	Memory A Data at 320MHz
MEM	W28	MDATA(26)	BIDIR	Memory A Data at 320MHz
MEM	W29	MDATA(25)	BIDIR	Memory A Data at 320MHz
VIDEO	Y 1	XTAL(1)	BIDIR	External crystal connections
MEM	Y 2	MDATB(62)	BIDIR	Memory B Data at 320MHz
MEM	Y 3	MDATB(59)	BIDIR	Memory B Data at 320MHz
MEM	Y 4	MDATB(63)	BIDIR	Memory B Data at 320MHz
POWER	Y 5	PLLVAA_1	POWER	PLL analogue power 3.3v

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	Y25	MDATA(21)	BIDIR	Memory A Data at 320MHz
MEM	Y26	MDQA(3)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	Y27	MDATA(22)	BIDIR	Memory A Data at 320MHz
MEM	Y28	SSTLVP(6)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	Y29	MDATA(23)	BIDIR	Memory A Data at 320MHz

8.2 Pinlist by Name

The table below provides a brief description of each pin. It is organized alphabetically by pin name. The block of GND pins from M12 to V18 is not included - these are listed in section 8.3, *Ground Connections*.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AE22	AGPADSTB(0)	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AGP	AF16	AGPADSTB(1)	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AGP	AG23	AGPADSTBN[0]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGP	AG16	AGPADSTBN[1]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGP	AH10	AGPPIPEN	OUT	PIPE#-Pipelined request(agp only)[3.3V]
AGP	AE11	AGPRBFN	BIDIR	RGF# Read buffer full (AGP only) (3.3v)
AGP	AF12	AGPSBA(0)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AF11	AGPSBA(2)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AE13	AGPSBA(4)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AF13	AGPSBA(5)	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGP	AG12	AGPSBA[1]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AJ12	AGPSBA[3]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AG13	AGPSBA[6]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AH13	AGPSBA[7]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGP	AH12	AGPSBSTB	OUT	SB_STB Sideband strobe (agp only)-(differential in AGP4x)[1.5V-3.3V]
AGP	AE12	AGPSBSTBN	OUT	SB_STB# Sideband strobe (agp only) differential strobe used in agp4x only (1.5v).
AGP	AF10	AGPST(0)	BIDIR	ST Status bus (agp only) (3.3v)
AGP	AJ10	AGPST[1]	BIDIR	ST Status bus(agp only)[3.3V]
AGP	AG11	AGPST[2]	BIDIR	ST Status bus (agp only) [3.3V]
AGP	AF18	AGPV3(1)	BIDIR	AGP I/O Reference voltage = VCCA 15/2(1.67v or 0.75v)

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AH22	AGPV3[0]	POWER	AGP pre-driver IO supply =3.3v
AGP	AJ14	AGPV3[2]	POWER	AGP pre-driver IO supply =3.3v
AGP	AH11	AGPV3[x]	POWER	AGP pre-driver IO supply =3.3v
AGP	AF25	AGPVREF	BIDIR	AGP I/O Reference voltage = VCCA 15/2 (1.67v or 0.75v)
AGP	AJ26	AGPZSET	IN	Analog reference impedance(resistor)-connect to VDDQ via 37.5 ohms
VIDEO	AD 3	DACAG(0)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AC 2	DACAG(1)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AA 5	DACAG(2)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AA 3	DACAG(3)	POWER	DAC analogue ground = 0v (isolated from GND)
VIDEO	AB 3	DACCOMP	POWER	See DAC spec for details
VIDEO	AA 2	DACSFADJ	BIDIR	DAC full scale adjust - connect via 226 ohm resistor to ground.
VIDEO	AC 3	DACVAA(0)	POWER	DAC analogue power = 3.3v
VIDEO	AB 2	DACVAA_1	POWER	DAC analogue power = 3.3v
VIDEO	AB 4	DACVAA_2	POWER	DAC analogue power = 3.3v
VIDEO	AB 5	DACVREF	BIDIR	See DAC spec for details
VIDEO	A11	DFPINTERRUPT	IN	General purpose interrupt
AGP	AE 9	DMASIDEBAND(0)	IN	Private sideband port (Tie high if unused)
AGP	AG 9	DMASIDEBAND[1]	IN	Private sideband port(tie high if unused)
AGP	AH 9	DMASIDEBAND[2]	IN	Private sideband port(tie high if unused)
POWER	AA29	GND(2)	POWER	Core and IO ground supply = 0v
POWER	A25	GND(4)	POWER	Core and IO ground supply = 0v
POWER	A 9	GND(59)	POWER	Core and IO ground supply = 0v
POWER	A21	GND(6)	POWER	Core and IO ground supply = 0v
POWER	E 1	GND(63)	POWER	Core and IO ground supply = 0v
POWER	AA 1	GND(65)	POWER	Core and IO ground supply = 0v
POWER	E29	GND0	POWER	Core and IO ground supply = 0v
POWER	A 5	GND01	POWER	Core and IO ground supply = 0v
POWER	J29	GND1	POWER	Core and IO ground supply = 0v
POWER	AJ17	GND29	POWER	Core and IO ground supply = 0v
POWER	AE29	GND3	POWER	Core and IO ground supply = 0v
POWER	AJ25	GND5	POWER	Core and IO ground supply = 0v
POWER	AJ13	GND51	POWER	Core and IO ground supply = 0v
POWER	AJ 9	GND60	POWER	Core and IO ground supply = 0v
POWER	AJ 5	GND62	POWER	Core and IO ground supply = 0v

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	J 1	GND64	POWER	Core and IO ground supply = 0v
POWER	AE 1	GND66	POWER	Core and IO ground supply = 0v
POWER	AJ21	GND7	POWER	Core and IO ground supply = 0v
VIDEO	AF 2	KCLKIN	BIDIR	External K clock input
MEM	P25	MADDRA(0)	BIDIR	Memory A Address signal
MEM	P28	MADDRA(1)	BIDIR	Memory A Address signal
MEM	P27	MADDRA(2)	BIDIR	Memory A Address signal
MEM	P29	MADDRA(3)	BIDIR	Memory A Address signal
MEM	P26	MADDRA(4)	BIDIR	Memory A Address signal
MEM	L 2	MADDRB(0)	BIDIR	Memory B Address signal
MEM	L 1	MADDRB(1)	BIDIR	Memory B Address signal
MEM	J 3	MADDRB(10)	BIDIR	Memory B Address signal
MEM	J 2	MADDRB(11)	BIDIR	Memory B Address signal
MEM	L 3	MADDRB(2)	BIDIR	Memory B Address signal
MEM	L 5	MADDRB(3)	BIDIR	Memory B Address signal
MEM	K 2	MADDRB(4)	BIDIR	Memory B Address signal
MEM	K 4	MADDRB(5)	BIDIR	Memory B Address signal
MEM	K 1	MADDRB(6)	BIDIR	Memory B Address signal
MEM	K 3	MADDRB(7)	BIDIR	Memory B Address signal
MEM	K 5	MADDRB(8)	BIDIR	Memory B Address signal
MEM	J 4	MADDRB(9)	BIDIR	Memory B Address signal
MEM	U27	MBAA(0)	BIDIR	Memory A Bank Address signal
MEM	V29	MBAA(1)	BIDIR	Memory A Bank Address signal
MEM	G 4	MBAB(0)	BIDIR	Memory B Bank address signal
MEM	G 2	MBAB(1)	BIDIR	Memory B Bank address signal
MEM	U28	MCASA	BIDIR	Memory A Control signal
MEM	H 3	MCASB	BIDIR	Memory B Control Signal
MEM	U26	MCKEA	BIDIR	Memory A Control signal
MEM	G 3	MCKEB	BIDIR	Memory B Control signal
MEM	J 5	MCKLB	BIDIR	Memory B 160MHz inverted clock out
MEM	H 1	MCKLBN	BIDIR	Memory B 160MHz inverted clock out
MEM	T25	MCLKA	BIDIR	Memory A 160MHz Clock out
MEM	T26	MCLKAN	BIDIR	Memory A 160MHz Inverted Clock out
VIDEO	AF 1	MCLKIN	BIDIR	External M clock input
MEM	AG26	MDATA(1)	BIDIR	Memory A Data at 320MHz
MEM	AD27	MDATA(10)	BIDIR	Memory A Data at 320MHz
MEM	AD26	MDATA(11)	BIDIR	Memory A Data at 320MHz
MEM	AB25	MDATA(15)	BIDIR	Memory A Data at 320MHz
MEM	AB29	MDATA(16)	BIDIR	Memory A Data at 320MHz
MEM	AC26	MDATA(16)	BIDIR	Memory A Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	AC27	MDATA(16)	BIDIR	Memory A Data at 320MHz
MEM	AC28	MDATA(16)	BIDIR	Memory A Data at 320MHz
MEM	AA25	MDATA(17)	BIDIR	Memory A Data at 320MHz
MEM	AA28	MDATA(18)	BIDIR	Memory A Data at 320MHz
MEM	AA27	MDATA(19)	BIDIR	Memory A Data at 320MHz
MEM	AG27	MDATA(2)	BIDIR	Memory A Data at 320MHz
MEM	AA26	MDATA(20)	BIDIR	Memory A Data at 320MHz
MEM	Y25	MDATA(21)	BIDIR	Memory A Data at 320MHz
MEM	Y27	MDATA(22)	BIDIR	Memory A Data at 320MHz
MEM	Y29	MDATA(23)	BIDIR	Memory A Data at 320MHz
MEM	W27	MDATA(24)	BIDIR	Memory A Data at 320MHz
MEM	W29	MDATA(25)	BIDIR	Memory A Data at 320MHz
MEM	W28	MDATA(26)	BIDIR	Memory A Data at 320MHz
MEM	W26	MDATA(27)	BIDIR	Memory A Data at 320MHz
MEM	V26	MDATA(28)	BIDIR	Memory A Data at 320MHz
MEM	F2	MDATA(29)	BIDIR	Memory A Data at 320MHz
MEM	V27	MDATA(29)	BIDIR	Memory A Data at 320MHz
MEM	AF26	MDATA(3)	BIDIR	Memory A Data at 320MHz
MEM	V25	MDATA(30)	BIDIR	Memory A Data at 320MHz
MEM	V28	MDATA(31)	BIDIR	Memory A Data at 320MHz
MEM	N28	MDATA(32)	BIDIR	Memory A Data at 320MHz
MEM	N27	MDATA(33)	BIDIR	Memory A Data at 320MHz
MEM	M29	MDATA(34)	BIDIR	Memory A Data at 320MHz
MEM	M25	MDATA(35)	BIDIR	Memory A Data at 320MHz
MEM	M28	MDATA(36)	BIDIR	Memory A Data at 320MHz
MEM	M27	MDATA(37)	BIDIR	Memory A Data at 320MHz
MEM	M26	MDATA(38)	BIDIR	Memory A Data at 320MHz
MEM	L26	MDATA(39)	BIDIR	Memory A Data at 320MHz
MEM	AG28	MDATA(4)	BIDIR	Memory A Data at 320MHz
MEM	L27	MDATA(40)	BIDIR	Memory A Data at 320MHz
MEM	L25	MDATA(41)	BIDIR	Memory A Data at 320MHz
MEM	K28	MDATA(42)	BIDIR	Memory A Data at 320MHz
MEM	K26	MDATA(43)	BIDIR	Memory A Data at 320MHz
MEM	K29	MDATA(44)	BIDIR	Memory A Data at 320MHz
MEM	K27	MDATA(45)	BIDIR	Memory A Data at 320MHz
MEM	K25	MDATA(46)	BIDIR	Memory A Data at 320MHz
MEM	J26	MDATA(47)	BIDIR	Memory A Data at 320MHz
MEM	H26	MDATA(48)	BIDIR	Memory A Data at 320MHz
MEM	H27	MDATA(49)	BIDIR	Memory A Data at 320MHz
MEM	AF27	MDATA(5)	BIDIR	Memory A Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	H28	MDATA(50)	BIDIR	Memory A Data at 320MHz
MEM	H25	MDATA(51)	BIDIR	Memory A Data at 320MHz
MEM	G27	MDATA(52)	BIDIR	Memory A Data at 320MHz
MEM	G26	MDATA(53)	BIDIR	Memory A Data at 320MHz
MEM	G28	MDATA(54)	BIDIR	Memory A Data at 320MHz
MEM	F26	MDATA(55)	BIDIR	Memory A Data at 320MHz
MEM	F29	MDATA(56)	BIDIR	Memory A Data at 320MHz
MEM	E26	MDATA(57)	BIDIR	Memory A Data at 320MHz
MEM	E27	MDATA(58)	BIDIR	Memory A Data at 320MHz
MEM	E28	MDATA(59)	BIDIR	Memory A Data at 320MHz
MEM	AF28	MDATA(6)	BIDIR	Memory A Data at 320MHz
MEM	D27	MDATA(60)	BIDIR	Memory A Data at 320MHz
MEM	D28	MDATA(61)	BIDIR	Memory A Data at 320MHz
MEM	D29	MDATA(62)	BIDIR	Memory A Data at 320MHz
MEM	C28	MDATA(63)	BIDIR	Memory A data at 320MHz
MEM	AF29	MDATA(7)	BIDIR	Memory A Data at 320MHz
MEM	AD29	MDATA(8)	BIDIR	Memory A Data at 320MHz
MEM	AD28	MDATA(9)	BIDIR	Memory A Data at 320MHz
MEM	AH27	MDATA[0]	BIDIR	Memory A data at 320MHz
MEM	B10	MDATB(0)	BIDIR	Memory B Data at 320MHz
MEM	D10	MDATB(1)	BIDIR	Memory B data at 320MHz
MEM	E 8	MDATB(10)	BIDIR	Memory B Data at 320MHz
MEM	C 7	MDATB(11)	BIDIR	Memory B Data at 320MHz
MEM	D 7	MDATB(12)	BIDIR	Memory B data at 320MHz
MEM	B 7	MDATB(13)	BIDIR	Memory B Data at 320MHz
MEM	D 6	MDATB(14)	BIDIR	Memory B data at 320MHz
MEM	C 6	MDATB(15)	BIDIR	Memory B Data at 320MHz
MEM	C 5	MDATB(16)	BIDIR	Memory B Data at 320MHz
MEM	B 5	MDATB(17)	BIDIR	Memory B Data at 320MHz
MEM	A 4	MDATB(18)	BIDIR	Memory B Data at 320MHz
MEM	B 4	MDATB(19)	BIDIR	Memory B Data at 320MHz
MEM	A10	MDATB(2)	BIDIR	Memory B Data at 320MHz
MEM	C 4	MDATB(20)	BIDIR	Memory B Data at 320MHz
MEM	B 3	MDATB(21)	BIDIR	Memory B Data at 320MHz
MEM	D 4	MDATB(22)	BIDIR	Memory B data at 320MHz
MEM	C 3	MDATB(23)	BIDIR	Memory B Data at 320MHz
MEM	D 1	MDATB(24)	BIDIR	Memory B data at 320MHz
MEM	E 2	MDATB(25)	BIDIR	Memory B Data at 320MHz
MEM	E 3	MDATB(26)	BIDIR	Memory B Data at 320MHz
MEM	E 4	MDATB(27)	BIDIR	Memory B Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	F 1	MDATB(28)	BIDIR	Memory B Data at 320MHz
MEM	C10	MDATB(3)	BIDIR	Memory B Data at 320MHz
MEM	F 3	MDATB(30)	BIDIR	Memory B Data at 320MHz
MEM	F 4	MDATB(31)	BIDIR	Memory B Data at 320MHz
MEM	M 5	MDATB(32)	BIDIR	Memory B Data at 320MHz
MEM	M 1	MDATB(34)	BIDIR	Memory B Data at 320MHz
MEM	M 2	MDATB(35)	BIDIR	Memory B Data at 320MHz
MEM	N 3	MDATB(35)	BIDIR	Memory B Data at 320MHz
MEM	N 4	MDATB(36)	BIDIR	Memory B Data at 320MHz
MEM	N 5	MDATB(37)	BIDIR	Memory B Data at 320MHz
MEM	N 1	MDATB(38)	BIDIR	Memory B Data at 320MHz
MEM	N 2	MDATB(39)	BIDIR	Memory B Data at 320MHz
MEM	E10	MDATB(4)	BIDIR	Memory B Data at 320MHz
MEM	P 5	MDATB(40)	BIDIR	Memory B Data at 320MHz
MEM	P 3	MDATB(41)	BIDIR	Memory B Data at 320MHz
MEM	P 2	MDATB(42)	BIDIR	Memory B Data at 320MHz
MEM	R 4	MDATB(43)	BIDIR	Memory B Data at 320MHz
MEM	R 5	MDATB(44)	BIDIR	Memory B Data at 320MHz
MEM	R 3	MDATB(45)	BIDIR	Memory B Data at 320MHz
MEM	R 2	MDATB(46)	BIDIR	Memory B Data at 320MHz
MEM	R 1	MDATB(47)	BIDIR	Memory B Data at 320MHz
MEM	T 5	MDATB(48)	BIDIR	Memory B Data at 320MHz
MEM	U 5	MDATB(49)	BIDIR	Memory B Data at 320MHz
MEM	D 9	MDATB(5)	BIDIR	Memory B data at 320MHz
MEM	U 1	MDATB(50)	BIDIR	Memory B Data at 320MHz
MEM	U 4	MDATB(51)	BIDIR	Memory B Data at 320MHz
MEM	U 2	MDATB(52)	BIDIR	Memory B Data at 320MHz
MEM	U 3	MDATB(53)	BIDIR	Memory B Data at 320MHz
MEM	V 1	MDATB(54)	BIDIR	Memory B Data at 320MHz
MEM	V 5	MDATB(55)	BIDIR	Memory B Data at 320MHz
MEM	V 4	MDATB(56)	BIDIR	Memory B Data at 320MHz
MEM	W 4	MDATB(57)	BIDIR	Memory B Data at 320MHz
MEM	W 2	MDATB(58)	BIDIR	Memory B Data at 320MHz
MEM	Y 3	MDATB(59)	BIDIR	Memory B Data at 320MHz
MEM	C 9	MDATB(6)	BIDIR	Memory B Data at 320MHz
MEM	W 3	MDATB(60)	BIDIR	Memory B Data at 320MHz
MEM	W 5	MDATB(61)	BIDIR	Memory B Data at 320MHz
MEM	Y 2	MDATB(62)	BIDIR	Memory B Data at 320MHz
MEM	Y 4	MDATB(63)	BIDIR	Memory B Data at 320MHz
MEM	B 9	MDATB(7)	BIDIR	Memory B Data at 320MHz

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	C 8	MDATB(8)	BIDIR	Memory B Data at 320MHz
MEM	B 8	MDATB(9)	BIDIR	Memory B Data at 320MHz
MEM	T28	MDDRA(10)	BIDIR	Memory A Address signal
MEM	T27	MDDRA(11)	BIDIR	Memory A Address signal
MEM	R29	MDDRA(5)	BIDIR	Memory A Address signal
MEM	R28	MDDRA(6)	BIDIR	Memory A Address signal
MEM	R26	MDDRA(7)	BIDIR	Memory A Address signal
MEM	R25	MDDRA(8)	BIDIR	Memory A Address signal
MEM	R26	MDDRA(9)	BIDIR	Memory A Address signal
MEM	AE26	MDMA(1)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	AB26	MDMA(2)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	W25	MDMA(3)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	N26	MDMA(4)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	L29	MDMA(5)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	H29	MDMA(6)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	F28	MDMA(7)	BIDIR	Memory A Data Write Masks at 320MHz
MEM	AJ27	MDMA[0]	BIDIR	Memory A Data write masks at 320MHz
VIDEO	E11	MDMB(0)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 8	MDMB(1)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 5	MDMB(2)	BIDIR	Memory B data writemasks at 320MHz
MEM	D 2	MDMB(3)	BIDIR	Memory B data writemasks at 320MHz
MEM	M 3	MDMB(4)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	P 4	MDMB(5)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	T 2	MDMB(6)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	V 3	MDMB(7)	BIDIR	Memory B Data Write Masks at 320MHz
MEM	AE28	MDQA(1)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	AB28	MDQA(2)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	Y26	MDQA(3)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	N25	MDQA(4)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	L28	MDQA(5)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	J27	MDQA(6)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	F27	MDQA(7)	BIDIR	Memory A 160MHz bi-directional strobe
MEM	AH26	MDQA[0]	BIDIR	Memory A 160MHz bir-directional strobe
MEM	C11	MDQB(0)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	E 9	MDQB(1)	BIDIR	Memory B 160MHz bidirectional strobe
MEM	B 6	MDQB(2)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	C 2	MDQB(3)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	L 4	MDQB(4)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	P 1	MDQB(5)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	T 4	MDQB(6)	BIDIR	Memory B 160MHz bi-directional strobe

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
MEM	V 2	MDQB(7)	BIDIR	Memory B 160MHz bi-directional strobe
MEM	T29	MDSFA	BIDIR	Memory A Control Signal
MEM	H 4	MDSFB	BIDIR	Memory B Control Signal
MEM	U29	MRASA	BIDIR	Memory A Control signal
MEM	H 2	MRASB	BIDIR	Memory B Control Signal
MEM	U25	MWEA	BIDIR	Memory A Control signal
MEM	H 5	MWEB	BIDIR	Memory B Control Signal
POWER	A 1	NC[1]		
POWER	AH 2	NC[10]	N/C	No-connect pins
POWER	A 2	NC[2]		
POWER	B 1	NC[3]		
POWER	B 2	NC[4]		
POWER	A28	NC[5]		
POWER	B28	NC[7]		
POWER	A29	NC[6]		
POWER	B29	NC[8]		
POWER	AG 3	NC[11]	N/C	No-connect pins
POWER	AJ 2	NC[12]	N/C	No-connect pins
POWER	AH28	NC[13]	N/C	No-connect pins
POWER	AH29	NC[14]	N/C	No-connect pins
POWER	AJ28	NC[15]	N/C	No-connect pins
POWER	AJ29	NC[16]	N/C	No-connect pins
POWER	AG 2	NC[9]	N/C	No-connect pins
AGP	AG25	PCIAD(0)	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AGP	AH25	PCIAD(1)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE21	PCIAD(10)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH21	PCIAD(11)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG21	PCIAD(12)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF21	PCIAD(13)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE20	PCIAD(14)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG20	PCIAD(15)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG18	PCIAD(16)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG17	PCIAD(17)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF17	PCIAD(19)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE18	PCIAD(20)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE16	PCIAD(21)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH17	PCIAD(22)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH16	PCIAD(23)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH15	PCIAD(24)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG15	PCIAD(25)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
AGP	AE15	PCIAD(26)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG14	PCIAD(27)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF14	PCIAD(28)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF15	PCIAD(29)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH24	PCIAD(3)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH14	PCIAD(30)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AE14	PCIAD(31)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AG24	PCIAD(4)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF24	PCIAD(5)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AH23	PCIAD(6)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF23	PCIAD(7)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AF22	PCIAD(8)	BIDIR	AD(31-0) address and data bus (1.5-3.3v)
AGP	AJ18	PCIAD[18]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
AGP	AJ24	PCIAD[2]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
AGP	AJ22	PCIAD[9]	BIDIR	AD{31:0) Address and data bus[1.5-3.3v)
AGP	AG22	PCICBEN[0]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AGP	AJ20	PCICBEN[1]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AGP	AH18	PCICBEN[2]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AGP	AJ16	PCICBEN[3]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AGP	AF 8	PCICLK	IN	Clk PciClk (3.3-5v)
AGP	AJ 8	PCICLKSEL	IN	Clock select-used to set config capabilities bit
AGP	AH19	PCIDEVSELN	BIDIR	DEVSEL# Device select[1.5V-3.3V]
AGP	AG 8	PCIFIFOINDIS	BIDIR	Private sideband port(input in test/config only)-leave open if unused
AGP	AH 8	PCIFIFOOUTDIS	BIDIR	Private sideband port(input in testconfig only)-leave open if unused
AGP	AE19	PCIFRAMEN	BIDIR	Frame# Cycle Frame(3.3v)
AGP	AE10	PCIGNTN	IN	Gnt# Grant (3.3v)
AGP	AE17	PCIIDSEL	IN	
AGP	AF 9	PCIINTAN	OUT	INTA# Interrupt A open drain
AGP	AF19	PCIIRDYN	BIDIR	IRDY# Initiator ready (3.3v)
AGP	AF20	PCIPAR	BIDIR	PAR Parity (3.3v)
AGP	AG10	PCIREQN	OUT	REQ# Request[3.3v]
AGP	AE 8	PCIRSTN	IN	RST# Reset (3.3v)
AGP	AH20	PCISTOPN	BIDIR	STOP# [3.3v]
AGP	AG19	PCITRDYN	BIDIR	TRDY# Target Ready[3.3v]

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	AJ 1	PLLAG_0	POWER	PLL analogue ground = 0v (islolated from GND)
VIDEO	AA 4	PLLAG_1	POWER	PLL analogue ground = 0v (isolated from GND)
VIDEO	AG 5	PLLDISABLE	IN	Disable PLL's
VIDEO	AH 1	PLLVAA_	POWER	PLL analogue power = 3.3v
POWER	Y 5	PLLVAA_1	POWER	PLL analogue power 3.3v
VIDEO	AH 3	RENDERSYNCN	BIDIR	Rasterizer resync for multichip solutions(core)
VIDEO	AH 6	ROMOEN	OUT	ROM Output Enable(active low)
VIDEO	AG 6	ROMSELECTN	OUT	ROM Select(active low)
VIDEO	AF 6	ROMWEN	OUT	ROM write enable (active low)
VIDEO	AH 7	SBCLK	BIDIR	
VIDEO	AF 7	SBDATA	BIDIR	
VIDEO	AF 3	SCLKIN	BIDIR	External M clock input
MEM	T 3	SSTLVP(0)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	M 4	SSTLVP(1)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	D 3	SSTLVP(2)	BIDIR	SSTL Class 1 Pre-driver IO supply =2.5v
MEM	A 8	SSTLVP(3)	POWER	SSTL Class 1 pre-driverIO supply = 2.5v
MEM	J25	SSTLVP(4)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	N29	SSTLVP(5)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	Y28	SSTLVP(6)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	AE27	SSTLVP(7)	POWER	SSTL Class 1 Pre-driver IO supply = 2.5v
MEM	T 1	SSTLVREF(0)	POWER	SSTL Class 1 IO reference voltage = VCCS25/2 = 1.25v
MEM	A 6	SSTLVREF(1)	POWER	SSTL Class 1 I/O reference voltage = VCCS25_2 = 1.25v
MEM	J28	SSTLVREF(2)	POWER	SSTL Class 1 IO reference voltage = VCCS25/2 = 1.25v
MEM	AB27	SSTLVREF(3)	POWER	SSTL Class 1 I/O reference voltage = VCCS25_2 = 1.25v
VIDEO	AE 2	TCLKIN	BIDIR	External T clock Input
AGP	AD 2	TESTMODE	IN	Production test global enable (Active high)
AGP	AH 4	TESTSELECT[0]	IN	Production test mode select
AGP	AJ 4	TESTSELECT[1]	IN	Production test mode select
AGP	AH 5	TESTSELECT[2]	IN	Production test mode select
AGP	AG 4	TEXTUREDOWNLOADINT	OUT	Texture download interrupt.
POWER	AJ23	VCCA15_4_0	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	AJ19	VCCA15_4_1	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
POWER	AJ15	VCCA15_4_2	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
POWER	AJ11	VCCA15_4_3	POWER	AGP interface VDDQ voltage level = 3.3v or 1.5v
POWER	AG 1	VCCS25_1_	POWER	SSTL IO driver supply (VCC) = 2.5v
POWER	A 3	VCCS25_1_0	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	AC 4	VCCS25_1_1	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	C 1	VCCS25_1_2	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	G 1	VCCS25_1_3	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	G29	VCCS25_1_3	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	C29	VCCS25_3_0	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	AC29	VCCS25_3_2	POWER	SSTL I/O Driver supply (VCC)=2.5v
POWER	AG29	VCCS25_3_3	POWER	SSTL IO driver supply (VCC) = 2.5v
POWER	AJ 3	VCCT33_0_	POWER	TTL IO driver supply (VCC) = 3.3v
POWER	AJ 7	VCCT33_0_	POWER	TTL IO driver supply (VCC) = 3.3v
POWER	A27	VCCT33_2_0	POWER	TTL I/O Driver supply (VCC)=3.3v
POWER	A23	VCCT33_2_1	POWER	TTL I/O Driver supply (VCC)=3.3v
POWER	A 7	VCCT33_2_2	POWER	TTL I/O Driver supply (VCC)=3.3v
VIDEO	AE 3	VCLKIN	BIDIR	Production test V clock Input
POWER	E23	VDD0	POWER	Core logic power = 1.8v
POWER	E24	VDD1	POWER	Core logic power = 1.8v
POWER	E 5	VDD10	POWER	Core logic power = 1.8v
POWER	E 6	VDD11	POWER	Core logic power = 1.8v
POWER	E 7	VDD12	POWER	Core logic power = 1.8v
POWER	F 5	VDD13	POWER	Core logic power = 1.8v
POWER	G 5	VDD14	POWER	Core logic power = 1.8v
POWER	AC 5	VDD15	POWER	Core logic power = 1.8v
POWER	AD 5	VDD16	POWER	Core logic power = 1.8v
POWER	AE 5	VDD17	POWER	Core logic power = 1.8v
POWER	AE 6	VDD18	POWER	Core logic power = 1.8v
POWER	AE 7	VDD19	POWER	Core logic power = 1.8v
POWER	E25	VDD2	POWER	Core logic power = 1.8v
POWER	F25	VDD3	POWER	Core logic power = 1.8v
POWER	G25	VDD4	POWER	Core logic power = 1.8v
POWER	AC25	VDD5	POWER	Core logic power = 1.8v
POWER	AD25	VDD6	POWER	Core logic power = 1.8v
POWER	AE23	VDD7	POWER	Core logic power = 1.8v
POWER	AE24	VDD8	POWER	Core logic power = 1.8v

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
POWER	AE25	VDD9	POWER	Core logic power = 1.8v
VIDEO	AB 1	VIDBLUE	BIDIR	Analogue blue component
VIDEO	AF 5	VIDDDCCLK	BIDIR	
VIDEO	AJ 6	VIDDDCDATA	BIDIR	
VIDEO	AF 4	VIDEOEXTCTRL	BIDIR	Input only as config
VIDEO	B11	VIDEOMERGEBLANK	BIDIR	DFPBlank or Merge blank input only for config
VIDEO	C13	VIDEOMERGECLOCK	BIDIR	Used for locking PLLs in multi-chip configurations - tie off if unused
VIDEO	B13	VIDEOMERGEDATA0	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B15	VIDEOMERGEDATA10	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C15	VIDEOMERGEDATA11	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E15	VIDEOMERGEDATA12	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B16	VIDEOMERGEDATA14	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C16	VIDEOMERGEDATA15	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E16	VIDEOMERGEDATA16	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A16	VIDEOMERGEDATA18	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B17	VIDEOMERGEDATA19	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A13	VIDEOMERGEDATA2	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A17	VIDEOMERGEDATA20	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E17	VIDEOMERGEDATA21	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D17	VIDEOMERGEDATA22	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C17	VIDEOMERGEDATA23	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A18	VIDEOMERGEDATA24	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B18	VIDEOMERGEDATA25	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	E18	VIDEOMERGEDATA 26	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C18	VIDEOMERGEDATA 27	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D18	VIDEOMERGEDATA 28	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D19	VIDEOMERGEDATA 29	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E13	VIDEOMERGEDATA 3	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B19	VIDEOMERGEDATA 30	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A19	VIDEOMERGEDATA 31	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C19	VIDEOMERGEDATA 32	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E19	VIDEOMERGEDATA 33	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B20	VIDEOMERGEDATA 34	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D20	VIDEOMERGEDATA 35	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A20	VIDEOMERGEDATA 36	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C20	VIDEOMERGEDATA 37	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E20	VIDEOMERGEDATA 38	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D21	VIDEOMERGEDATA 39	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E14	VIDEOMERGEDATA 4	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C21	VIDEOMERGEDATA 40	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B21	VIDEOMERGEDATA 41	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E21	VIDEOMERGEDATA 42	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A22	VIDEOMERGEDATA 43	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D22	VIDEOMERGEDATA 44	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	C22	VIDEOMERGEDATA 45	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B22	VIDEOMERGEDATA 46	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	E22	VIDEOMERGEDATA 47	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C23	VIDEOMERGEDATA 48	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D13	VIDEOMERGEDATA 48	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D23	VIDEOMERGEDATA 49	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B14	VIDEOMERGEDATA 5	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B23	VIDEOMERGEDATA 50	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D24	VIDEOMERGEDATA 51	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C24	VIDEOMERGEDATA 52	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D14	VIDEOMERGEDATA 52	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B24	VIDEOMERGEDATA 53	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A24	VIDEOMERGEDATA 54	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D25	VIDEOMERGEDATA 55	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C25	VIDEOMERGEDATA 56	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D15	VIDEOMERGEDATA 56	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B25	VIDEOMERGEDATA 57	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A26	VIDEOMERGEDATA 58	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B26	VIDEOMERGEDATA 59	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C14	VIDEOMERGEDATA 6	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C26	VIDEOMERGEDATA 60	BIDIR	Merge (64 bits) and DFP data (60 bits) config.

GROUP	BGA PAD	PIN NAME	TYPE	DESCRIPTION
VIDEO	D16	VIDEOMERGEDATA 60	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	B27	VIDEOMERGEDATA 61	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D26	VIDEOMERGEDATA 62	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	C27	VIDEOMERGEDATA 63	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A14	VIDEOMERGEDATA 7	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	A15	VIDEOMERGEDATA 9	BIDIR	Merge (64 bits) and DFP data (60 bits) config.
VIDEO	D11	VIDEOMERGEDATA STROBEOUT	OUT	Strobe for merge data and dFP
VIDEO	A12	VIDEOMERGEHSYN CN	BIDIR	Horizontal strobe used in multichip configs (tie off if unused)
VIDEO	D12	VIDEOMERGESTRO BEIN(0)	IN	Used for multi-chip solutions - tie unused low
VIDEO	C12	VIDEOMERGESTRO BEIN(1)	IN	Used for multichip solutions - tie unused low.
VIDEO	B12	VIDEOMERGESTRO BEIN(2)	IN	Used for multichip solutions - tie unused low.
VIDEO	E12	VIDEOMERGEVSYN CN	BIDIR	Vertical strobe used I multiple chip configs. Tie off if unused.
VIDEO	AC 1	VIDGREEN	BIDIR	Analogue green component
VIDEO	AE 4	VIDHSYNC	OUT	DAC Horizontal sync
MEM	AD 1	VIDRED	BIDIR	Analogue green component
VIDEO	AG 7	VIDRIGHTEYE	BIDIR	Right eye signal for stereo/config bit
VIDEO	AD 4	VIDVSYNC	BIDIR	DAC Vertical sync/config bit
VIDEO	Y 1	XTAL(1)	BIDIR	External crystal connections
VIDEO	W 1	XTAL(2)	BIDIR	External Crystal connection

8.3 Ground Connections

GND designates pins where core and IO ground supply = 0v

The following pins are GND: AJ5, A5, A9, A21, A25, AA1, AA29, AE1, AE29, AJ21, AJ25, AJ5, AJ9, E1, E29, J1, J29, M12, M13, M14, M15, M16, M17, M18, N12, N13, N14, N15, N16, N17, N18, P12, P13, P14, P15, P16, P17, P18, R12, R13, R14, R15, R16, R17, R18, T12, T13, T14, T15, T16, T17, T18, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V18

8.4 Schematics

The following pages contain a typical set of GLINT R5 schematics for a single-processor board with 64MB of DDR memory. These schematics are supplied for illustration purposes only and are neither specifications nor working drawings.[1]

[1] If viewing this document on screen, insert schematics from the separate drawing bundle on the blank pages following.

9

Memory System

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The GLINT R5 memory system is intended for use with Synchronous Dynamic Memories. The memories can be SGRAM or SDRAM devices and both single- and double- data rate devices are supported. Configuration for SDR or DDR is via pull-up or pull-down resistors on pins:

Pin Name	Function
VideoMergeData14	DDR Enable (0=SDR)
VideoMergeData15	Use common strobes (DDR SGRAMS, active = high)
VideoMergeData16	Use internal strobes (SDRAMS, active = high)

Table 9.1 Configuration Pins

The system uses two distinct controllers, each of which supports up to 4 banks in one 64MB memory block. There is no ChipSelect parameter. Halfwidth is supported by simply disabling the B controller.

Each controller has its own Address Bus, Control Signals and full register set. This theoretically allows asymetric memory configurations or the use of different device types on each controller (not tested and not recommended). Data strobes are supplied per byte for DDR memories, but SDR SDRAMs do not use external strobes. and can be configured for:

- DDR SDRAM
- DDR SGRAM
- SDR SGRAM and SDRAM

9.1 Strobe Setup

Strobes are supplied from memory on data transitions and repositioned to bisect the data using delay chains. There is a register bitfield group for each strobe or byte enable (depending on device type). See below for a typical clock delay chain register.

Name	Type	Offset	Format
LocalMem1ADelayOut1	Memory Control Command register	0x10A0	Bitfield

Bits	Name	Read	Write	Reset	Description
0..3	StrobeDelay6	✓	✓	0	Bit code of delay: 0 = 0 taps, 15 = 15 taps
4	StrobeInvert6	✓	✓	0	0 = no invert 1 = invert
5..8	StrobeDelay7	✓	✓	0	Bit code of delay: 0 = 0 taps, 15 = 15 taps
9	StrobeInvert7	✓	✓	0	0 = no invert 1 = invert
10..13	ClockDelay	✓	✓	0	Bit code of delay: 0 = 0 taps, 15 = 15 taps
14	ClockInvert	✓	✓	0	0 = no invert 1 = invert
15..31	Reserved	✓	✗	0	

In each channel, a 5-bit delay field allows 0 to 15 delays of 1/4 ns each. The 5th bit allows strobe inversion, so the maximum delay = 1/2 clock plus 3-3/4 ns. Two adjacent registers (-0 and -1) are used to accommodate the full set of strobe and clock delays, with ClockDelay in the upper bits.

Note: There is no clock In delay

9.1.1 DDR SDRAM

This configuration uses a full set of 4 individual strobes plus clock out. There is one delay register for each byte lane and controller. The memory devices are 4-bank x 16 bit.

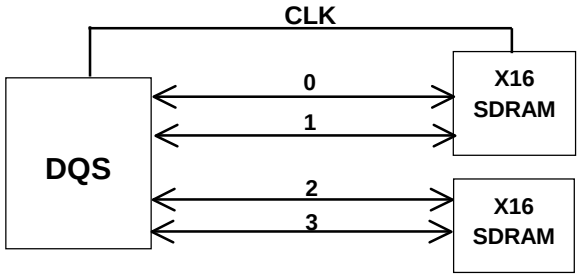


Figure 9.1 Non-common Strobes (DDR SDRAM)

9.1.2 DDR SGRAM

For sigle-strobe devices the strobe is replicated internally on input to supply the 4 strobe lines. DDR SGRAMs are not frequently encountered because they tend to use arbitrary blockfill without support for byte masking.

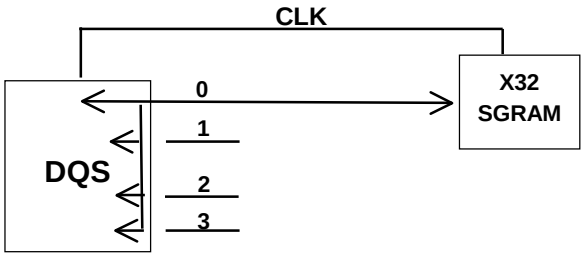


Figure 9.2 Common Strobes (DDR SGRAM)

9.1.3 SDR SDRAM and SGRAM

Single Data-rate devices use internal strobes as shown:

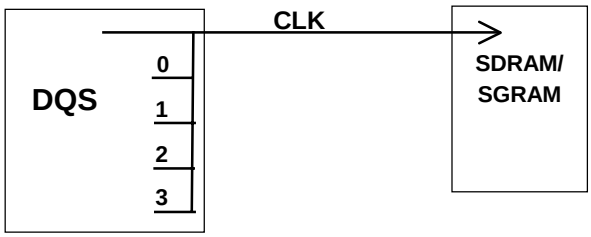


Figure 9.3 Internal Strobes (SDR SGRAM and SDRAM)

The diagrams show a single controller driving a device or devices which may have up to 4 banks in 1 block. Normally two controllers are used in a symmetric pair configuration, although symmetry is not strictly required. The maximum total configuration is 128Mbytes SDRAM or SGRAM, however configurations down to 2MB are supported.

The memory array requires no external logic and has been designed to deliver optimum performance on low cost boards by minimizing susceptibility to signal skew.

9.1 System Parameters

The Memory System employs a comprehensive set of registers which allow for a wide range of memory configurations. The timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on memory type, speed grade, data rate and the system clock frequency (MClk). Memory functionally can be

enabled depending on the type fitted. Full addressing control is available so that virtually any memory configuration can be fitted.

The following parameters are used to control accesses to the memory. These values fall into three categories

- Addressing
- Functionality and Optimizations
- Timing and Mode

9.1.1 Addressing

These parameters are specified in the **LocalMemCaps** registers

9.1.1.1 ColumnAddress (CAS)

This defines the number of address bits required to generate the column addresses for the memory devices fitted:

Address Bits	Parameter
8	0
9	1
10	2
11	3

9.1.1.2 RowAddress (RAS)

This defines the number of address bits required to generate the row addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet. For example RA8~RA0 therefore the Row Address parameter would be 9

Address Bits	Parameter
10	0
11	1
12	2

9.1.1.3 BankAddress

This parameter defines the number of address bits required to generate the bank addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

Banks	Parameter
2	0 (i.e. 1-bit address)
4	1 (i.e. 2-bit address)

9.1.1.4 PageSize

This parameter defines the address range for a memory page of the memory array fitted. The value can be calculated as (column address bits of device – 5).

9.1.1.5 RegionSize

This parameter defines the addressing range for each of the four page-detectors implemented in each memory controller. The minimum region a page-detector can be assigned to is one internal bank, the maximum is all of the memory fitted. There are some memory configurations where not all the page-detectors can be deployed, for example when three blocks of memory devices are used.

The region size value can be calculated as:

$$\mathrm{Log2}\left(\frac{\mathrm{TotalMemory}}{\mathrm{BytesperMemWidth} \times \mathrm{RegionsUsed}}\right) - 5$$

Where Total Memory = The total size of memory fitted in megabytes

Bytes per Memory Width = 16 (128 / 8)

Regions Used = (if total number of Banks (Blocks fitted)

Then Blocks Fitted

else Total Banks

)

This can be represented as a table:

Region Size	Parameter
16MB	15
8MB	14
4MB	13
2MB	12
1MB	11
Others	available

9.1.2 Functionality and Optimizations

These parameters are specified in the **LocalMemCaps** registers

9.1.2.1 NoPrechargeOpt

This flag when set will disable the back to back READ - PRECHARGE optimization, inserting clocks to the value of the CAS Latency between the commands. If the memory

devices fitted are capable of executing a READ command directly followed by a PRECHARGE command, this flag should be left clear for optimal performance.

9.1.2.2 SpecialModeOpt

This flag when set enables the memory controller to issue a Special Mode Register Set (SMRS) command, without regard to the current state of the internal banks of the SGRAM. Some memory devices require all internal banks to be in the same state before an SMRS command is issued. For these devices, ensure that the flag is cleared. The memory controller will issue a PRECHARGE command to the devices to ensure all internal banks are in the IDLE mode before issuing the SMRS command. If the memory devices fitted are capable of this function, optimally this flag should be set.

9.1.2.3 TwoColorBlockFill

This flag when set allows the memory controller to utilize the 2 internal Color Registers that some SGRAM devices are equipped with. If the memory devices fitted only have 1 Color Register, this flag should be cleared. When this flag is cleared the memory controller will fully emulate the two color fill operations.

9.1.2.4 NoWriteMask

This flag when set disables the memory controller from using the internal MASK Register of an SGRAM. This flag must be set if SDRAMS are fitted (and will generally be set for DDR SGRAMs). When set, the memory controller emulates write mask operation. This is only a partial emulation using the byte enables so bit precision is not achieved.

9.1.2.5 NoBlockFill

This flag when set disables the memory controller from issuing a Block Fill command to the memories. This flag must be set if SDRAMS are fitted. When this flag is set the memory controller will fully emulate the block fill operations.

9.1.2.6 NoLookAhead

This flag when set disables the memory controller from issuing command to one bank of memory, whilst another bank is in the process of PRECHARGHING. Nominally for performance, this flag should be left cleared.

9.1.3 Timing and Mode

These parameters are specified in the **LocalMemTiming** and **LocalMemControl** registers.

9.1.3.1 TurnOn (Write to Read transition)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ command to one block of memory devices to a READ of another Block. (Block to Block Read Delay). Two parameters from the memory device data sheet must be used to determine what value TurnOn must be set to. The timing parameter tHZ defines the tri-state time and the parameter tLZ defines the drive time of the device. If tLZ is greater than tHZ, then this parameter can safely be set to zero.

9.1.3.2 TurnOff (Read to Write transition)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ and a WRITE command (Read – Write turn around). This parameter is defined in the memory device data sheet, usually as tHZ.

9.1.3.3 RegisterLoad (RL)

This parameter defines the number of MClk cycles that need to be inserted between issuing a SMRS and another command. This parameter is usually detailed in the memory device data sheet as tRSC. If tRSC is quoted including the SMRS cycle, then RegisterLoad should be calculated as tRSC (in MClk cycles) – 1.

9.1.3.4 BlockWrite (BW)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCK WRITE and another command. This parameter is usually detailed in the memory device data sheet as tBWC. If tBWC is quoted including the SMRS cycle, then BlockWrite should be calculated as tBWC (in MClk cycles) – 1.

9.1.3.5 ActivateToCommand (ATC)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a command. This parameter is usually detailed in the memory device data sheet as tRCD. If tRCD is quoted including the ACTIVATE cycle, then *ActivateToCommand* should be calculated as tRCD (in MClk cycles) – 1.

9.1.3.6 BlockWriteToPrecharge (BTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCKWRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tBPL (tBWR). If tBPL is quoted including the BLOCKWRITE cycle, then BlockWriteToPrecharge should be calculated as tBPL (in MClk cycles) – 1.

9.1.3.7 WriteToPrecharge (WTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a WRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRDL (tWR). If tRDL is quoted including the WRITE cycle, then WriteToPrecharge should be calculated as tRDL (in MClk cycles) – 1.

9.1.3.8 ActivateToPrecharge (ATP)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRAS. If tRAS is quoted including the ACTIVATE cycle, then ActivateToPrecharge should be calculated as tRAS (in MClk cycles) – 1.

9.1.3.9 RefreshCycle (RC)

This parameter defines the number of MClk cycles that need to be inserted between issuing a REFRESH and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRC. If tRC is quoted including the REFRESH command cycle, then *RefreshCycle* should be calculated as tRC (in MClk cycles)/32 – 1. It must be enabled by setting the *Enable* bit in **LocalMemRefresh**

9.1.3.10 ActivateToActivate (ATA)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a subsequent ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRRD. If tRRD is quoted including the ACTIVATE cycle, then ActivateToActivate should be calculated as tRRd (in MClk cycles) – 1.

9.1.3.11 CasLatency (CL)

This parameter determines the CAS latency expected by the memory controller. The *CasLatency* parameter can be loaded directly with the appropriate value from the memory device data sheet plus 1. For example, if a CAS latency of 2 is required then the CasLatency parameter should be set to 3.

9.1.3.12 Interleave

Where the full complement of 64MB per controller is fitted, Interleave allows the banks on each controller to function as a single page. For example, controller A with 4-bank SDRs x 2k would, with Interleave enabled, function as a controller with one bank of 8k.

On some boards *Interleave* with 64MB RAM is set up to create a 128MB framebuffer (for Bypass operations) dispersed into 16MB chunks totalling 64MB. The chunks can be used and replicated for a variety of purposes depending on the API.

Boards may require a supplementary resistor to work properly in Interleave mode.

9.1.3.13 Mode

This parameter defines the value of the Mode Register loaded into the SGRAM or SDRAM at the end of the boot sequence. Bits 22 to 31 map to bits 0 to 9 of the Mode register.

Note: *Burst type should be sequential, burst length should be set to a value of one*[2] *and CAS latency should be consistent with the* CASLatency *parameter.*

For devices that have a ColorRegister *field, this should be consistent with the* ***TwoColorBlockFill*** *flag. All other bits in the Mode field should be set low.*

9.1.3.14 Extended Mode: Parameters

These fields control the DLL enables, Driver Impedance control (DIC) and QFC. DLL and DIC are enabled, QFC is disabled.

9.1.3.15 RefreshEnable

This flag should be set for Refresh commands to be issued by the memory controller.

9.1.3.16 RefreshCount

This parameter defines the period between AUTO-REFRESH commands being issued to the synchronous memories. The count is in ((MClks/32) + 16) i.e. if RefreshCount = 1, the synchronous memories will be refreshed every 48 MClk cycles. For the required refresh rate see the synchronous memory data sheet.

---

[2] With DDR devices, this value implies 2 accesses. With SDRs, it implies 1 access.

9.2 Example Parameter Values

The following device types and values are given as examples and should not be taken as recommendations.

9.2.1 128Mb x 32 DDR SDRAM - 64MB per Controller (4 Devices Per Controller)

Table 9.1 For a GLINT R5 device running 128Mb x 32 DDR SDRAM - 64MB per Controller

Parameter	Value (binary)	Comment
ColumnAddress	0001	9
RowAddress	0010	12
BankAddress	0001	2 bit Addr (4 Banks)
PageSize	0011	3 (256)
RegionSize	1111	15 (16 MB)
Interleave	0	Optional

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	SDRAM
NoWriteMask	1	SDRAM
NoBlockFill	1	SDRAM
NoLookAhead	0	Preferred

Configuration Resister	Value	Comment
DDR Enable	1 (High)	DDR Devices
Use common strobes	0 (Low)	SDRAM Unique DQS
Use internal strobes	0 (Low)	DDR Use External DQS

9.2.2 64Mb x 16 DDR SDRAM - 32MB per Controller (4 Devices Per Controller)

.

Table 9.2 64Mb x 16 DDR SDRAM - 32MB per Controller (4 Devices Per Controller)

Addressing Parameters	Value (binary)	Comment
ColumnAddress	0000	8
RowAddress	0010	12
BankAddress	0001	2 bit Addr (4 Banks)
PageSize	0010	2 (128)
RegionSize	1110	14 (8 MB)
Interleave	0	NA

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	SDRAM
NoWriteMask	1	SDRAM
NoBlockFill	1	SDRAM
NoLookAhead	0	Preferred

Configuration Resister	Value	Comment
DDR Enable	1 (High)	DDR Devices
Use common strobes	0 (Low)	SDRAM Unique DQS
Use internal strobes	0 (Low)	DDR Use External DQS

9.2.3 64Mb x 32 DDR SGRAM (Block Fill with No Column Mask, No Write per Bit) - 16MB per Controller (2 Devices Per Controller)

.

Table 9.3 64Mb x 32 DDR SGRAM (Block Fill with No Column Mask, No Write per Bit)

Addressing Parameters	Value (binary)	Comment
ColumnAddress	0000	8
RowAddress	0001	11
BankAddress	0001	2 bit Addr (4 Banks)
PageSize	0010	2 (128)
RegionSize	1101	13 (4 MB)
Interleave	0	NA

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	0	Required SMRS
TwoColorBlockFill	0	NA
NoWriteMask	1	NA
NoBlockFill	0	SGRAM (No Column Mask)
NoLookAhead	0	Preferred

Configuration Resister	Value	Comment
DDR Enable	1 (High)	DDR Devices
Use common strobes	1 (High)	SGRAM 1 DQS per device
Use internal strobes	0 (Low)	DDR Use External DQS

9.2.4 32Mb x 32 DDR SGRAM - 8MB per Controller (2 Devices Per Controller)

.

Table 9.3 64Mb x 32 DDR SGRAM (Block Fill with No Column Mask, No Write per Bit)

Addressing Parameters	Value (binary)	Comment
ColumnAddress	0000	8
RowAddress	0001	11
BankAddress	0000	1 bit Addr (2 Banks)
PageSize	0010	2 (128)
RegionSize	1101	13 (4 MB)
Interleave	0	NA

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	0	Required SMRS
TwoColorBlockFill	0	NA
NoWriteMask	0	SGRAM
NoBlockFill	0	SGRAM
NoLookAhead	0	Preferred

Configuration Resister	Value	Comment
DDR Enable	0 (Low)	SDR Devices
Use common strobes	0 (Low)	NA
Use internal strobes	0 (High)	SDR Use Internal Clock

10

Reset

Specific signal pins are read on the trailing edge of a reset and the values present (due to pull-ups or pull-downs) are used to initialized bits of particular registers. Most of the sampled values from the I/O pins are read into the **ChipConfig** register - for details refer to volume III. In some cases they do not - e.g. **CfgMaxLat** and **CfgMinGrant** which directly update hardware registers only.

During software bus reset both the bus master and the bus slave state machines continue to run. However, the Region Zero registers within the PCI bus interface are reset as will as the GP Input and Output FIFOs. Driver software must write to a PCI configuration register to disable the bus master before asserting a software reset. This ensures that the master is not trying to load the GP Input FIFO during such a reset.

Note: When bus retries are disabled the current implementation will accept and then discard all write accesses to the GP Input FIFO — this is different from the manner in which Bypass accesses are handled. The situation only occurs if driver sofware performs a soft reset and does not check that it has completed before writing to the FIFO.]

At chip reset the *BusMasterEnable* bit in the **CFGCommand** register must be set to allow DMA to operate.

10.1 Configuration Pins

A number of parameters for the bus interface are set at reset time: the reset state is configured using resistors connected to *configuration pins*. These pins normally form part of the pixel bus but are tri-state at reset. The state of these pins is sampled on the trailing edge of reset. The configuration pins are listed below and the associated register bits are described in Volume II of the *GLINT R5 Reference Guide*.

Most of the sampled values from these configuration pins are loaded into the **ChipConfig** register, on the trailing edge of reset. This register can then be read back over the PCI bus and modified by the host processor if required. **BaseAddress1Size** and **BaseAddress2Size** are not loaded into **ChipConfig** but feed directly to the PCI interface to define the sizes of Base Addresses 1 and 2.

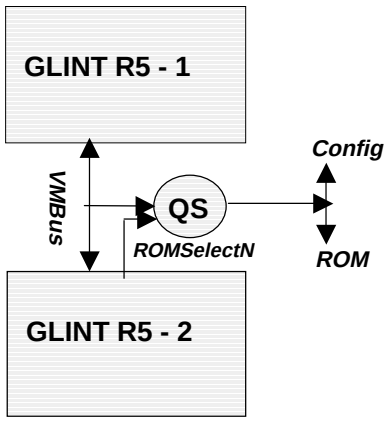
All internal functions which sample these values take them from the **ChipConfig** register. This allows boot time software to change the default power-on values where appropriate.

10.2 ROM support

R5 uses a Flash ROM to store code needed for device-specific initialization and the SVGA BIOS. This is configured via the **VideoMergeBus** pins and a QuickSwitch controlled via ROMSelectN (30pf) should be used to allow access to the ROM configuration or remove the load from the bus.

The pins used by the configuration resistors are shared with the address lines going to the ROM device. The bottom 32 bits of the merge bus are located behind the quickswitch to isolate the video merge bus from the ROM during normal video operation.

The ROM address lines are on **VideoMergeData** pins 0 to 15. The ROM data lines are on **VideoMergeData** pins 16 to 23 (these must not have config resistors fitted).
VideoMergeData pins 0 to 15 and 24 to 31 are available for config resistors.



The configuration pins are mapped to real device pins as follows:

Table 10- 1 Reset Signal Pins

Name	Pin	Description
BaseClassZero	VideoMergeData(0)	1 = force PCI Bass Class Code to be zero
VGAEnable	VidRightEye	1 = internal VGA subsystem present
VGAFixed	VideoMergeData (1)	1 = enable VGA fixed address decoding
VGANoAlias	VideoMergeData (2)	0 = 10 bit VGA I/O Decode (aliasing enabled) 1 = 32-bit VGA I/O Decode (aliasing disabled)
Retry Disable	VideoMergeData (3)	1 = Disable PCI Retry using "Disconnect Without Data"
ShortReset	VideoMergeData (4)	1 = generate short "AReset" pulse (BusReset + 64 clocks)
AGP1Xcapable	VideoMergeData (5)	1 = AGP 1Xcapable
AGP2Xcapable	VideoMergeData (6)	1 = AGP 2X Capable
AGP4Xcapable	VideoMergeData (7)	1 = AGP 4XCapable - this should never be set on an R5 unless 4X drivers are added
SBACapable	VideoMergeData (8)	1 = AGP Sideband AddressingCapable
SubsystemFromRom	DFPBlank	1 = Load subsystem Vendor ID and Subsystem ID from ROM. 0 = Leave as reset values
WCEnable	VideoMergeData (10)	0 = Upper half of region Zero is byte-swapped 1= Upper half of region Zero flagged internally as write-combined
PrefetchEnable	VideoMergeData (11)	1 = Base Address registers 1 and 2 marked as prefetchable
Alternate DeviceID	VidExtCtrl	0 = R5 device ID is 0x0012 1 = R5 device ID is 0x0013
AutoCalEnable	VideoMergeData (12)	0 = AutoCal disable 1 = AutoCal enable
DDR Enable	VideoMergeData (13)	0 = DDR Memory not fitted 1 = DDr Memory fitted
Common Strobes	VideoMergeData (14)	0 = MemConfig Common Strobes = false 1 = MemConfig Common Strobes = true
Internal Strobes	VideoMergeData (15)	0 = MemConfig Internal Strobes = false 1 = MemConfig Internal Strobes = true
ChipID(0-2)	PCIFIFOOutDis(bit0) PCIFIFOInDis(Bit1) VidVSync(bit2)	Sets the ID for this chip in a multi-chip adapter, starting at 0 for the primary and increasing by 1 as we move down the chain.

Name	Pin	Description
BaseAddress1 Size(0-2)	VideoMergeData (24-26)	Indicates the size of the PCI Base Address Region: 0 = not enabled 1 = 32MB 2 = 64MB 3 = 128MB 4...7 Reserved
BaseAddress2 Size(0-2)	VideoMergeData (27-29)	

A hard-wired configuration pin also exists (Table 10-2). **PCIClkSel** sets bit 5 of the **CFGStatus** register, which is Read-only.

Table 10-2 Hard Configuration Pin

Name	Pin	Description
PCIClk66	PCIClkSel	0 = up to 33MHz 1 = 66 MHz

10.3 RAMDAC Resets

RAMDAC signals are reset on either program soft resets or hard (power-on) reset, with exceptions. The following signals are reset following power-on only:

RDDClkSetup[1-2]
RDDClkControl
RDDClk0PreScale
RDDClk0FeedBackScale
RDDClk0PostScale
RDDClk1PreScale
RDDClk1FeedBackScale
RDDClk1PostScale
RDDClk2PreScale
RDDClk2FeedBackScale
RDDClk2PostScale
RDDClk3PreScale
RDDClk3FeedBackScale
RDDClk3PostScale
RDDKClkControl
RDKClkPreScale
RDKClkSetup[1-2]
RDKClkFeedBackScale
RDKClkPostScale
RDMClkControl
RDSClkControl
RDTClkControl
RDTClkPreScale
RDTClkFeedbackScale
RDTClkPostScale

Three phase locked loops (PLLs) are included in the RAMDAC unit, dedicated to generating DClk (Pixel clock) and a derived Video clock (VClk) as well as the Core and Timing (Kclk and TClk) Plls.

The DClk PLL has four sets of control registers (e.g. **RDDclk3Prescale**). The set selection is defined by two control bits from outside the unit.

The reset states for the DClk PLL control regsiters are:

Register set	Frequency
0	25.057MHz
1	28.278MHz
2	Undefined
3	Undefined

The KClk and TClk PLLs reset to approximately 50MHz. All figures assume a 14.31818MHz external reference.

An external signal can put the PLLs into bypass mode. In this mode Tclk, KClk and DClk are taken from pins and the PLLs have no effect.

11

Thermal

The maximum junction temperature must be kept below Tj(max)and this can only be guaranteed by proper analysis of the operating environment and the thermal path between the die and the air surrounding it.

Data shown below are provisional for R5 pending the availability of actual test results. A summary table for various installations is shown below, followed by the relevant equations for reference use.

	Thermal Resistance (deg.C/Watt) = θ_{ja}		
	0 m/s	***1 m/s***	***2 m/s***
No heatsink	10.9	9.1	7.7
Heatsink (37mm sq.x 2mm	9.2	7.2	6.2

Table 10-1 R5 Package (529 HSBGA) Thermal Performance

11.1 Device Characteristics

These are fixed characteristics of the device and are independent of the operating environment or the characteristics of any heatsink:-

Maximum Junction Temperature	$T_{j(max)}$	= 125 °C.
Maximum Power Dissipation (provisional)	Pd(max)	= 7 Watts
Nominal memory clock frequency	f_{MClk}	= 166 MHz
Nominal core clock frequency	f_{KClk}	= 200 MHz
Junction to top of case resistance (provisional)	θ_{jt}	= 1°C/Watt

11.2 Thermal Model

The formula used to calculate the junction temperature (Tj) for an ambient temperature of 40°C is:

$$\begin{aligned} Tj &= Ta + Pd\theta_{ja} \\ &= 40 + 7(10.9) \\ &= 116°C \end{aligned}$$

Where:

T_j = Junction temperature (°C)
T_a = Ambient temperature (°C)
P_d = Power dissipation (Watts)
θ_{jt} = Junction to top of case thermal resistance (°C/Watt)

θ_{cs} = Case to Heatsink
thermal resistance (°C/Watt)
θ_{sa} = Heatsink to Air
thermal resistance (°C/Watt)
θ_{ja} = Total Junction to Air thermal resistance (°C/Watt)

11.3 Cooling

GLINT R5 should not require an attached heatsink or fan when used in an ordinary office environment. If ambient temperatures are expected to routinely exceed 40° C then a heatsink may be fitted.

11.4 Operation with Heatsink

11.4.1 Heatsink Attachment

The following method has been approved for the purpose of attaching a heatsink directly onto the HSBGA package:

Thermally conductive epoxy using either Loctite Output 315 with Loctite 7386 or type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 95% coverage of the contact area.

Typical achievable θ_{cs} using this method is 1.0 ° C/Watt

11.4.2 Calculating cooling requirements

With a heatsink attached to the device the junction temperature will depend on θcs and θsa where θcs is the thermal resistance of the join between the heatsink and the case and θsa is the thermal resistance of the heatsink, which will be a function of system airflow.

Typically,

$Tj = Ta + Pd (\theta_{jt} + \theta_{cs} + \theta_{sa})$

Hence with no heatsink:at 55°C:

$Tj = 55 + 7*10.9 = 131.3$

…which is excessive. So a heatsink: having, e.g. $\theta_{sa} = 6$°C/W

$Tj = 55 + 7*(1+1+6) = 111$°C/W

…or a fan:

$Tj = 55 + 7*(1+1+3.5) = 93.5$°C/W

…is required

11.4.3 Temperature Range (Commercial/Embedded Applications)

R5 is operational in embedded use under a wide range of ambient air temperatures:

Operating Range: -55°C (no heatsink) to 88.5°C (heatsink and fan, 2m/s airflow)

Storage Range: -65°C to 150°C (suitably packed)

12 Electrical

Provisional values may be subject to change and should be checked against current values on the 3Dlabs website[3].

12.1 Absolute Maximum Ratings

Junction Temperature	125°C
Storage Temperature	-65°C to 150°C
VCC25 DC Supply Voltage	2.8V
VCC33 DC Supply Voltage	3.8V
VDD DC Supply Voltage	2.1V
I/O Pin Voltage with respect to GND	-0.5V to VCC3.3 + 0.5V

12.2 DC Specifications

Symbol	Parameter	Min	Max	Unit
VCC33	Supply Voltage	3.0	3.6	V
VCC25	Supply Voltage	2.25	2.75	V
VDD(1-8)	Supply Voltage	1.62	1.98	
LPIN	Pin Inductance		12	nH
ICC (3V)	Power Supply Current		1	A
ICC (2.5V)	Power Supply Current		1.4	A

12.2.1 PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage		0.8	V
V^{PIH}	Input High Voltage	2.0		V
V_{POL}	Output Low Voltage		0.5	V
V_{POH}	Output High Voltage	2.4		V
I_{PIL}	Input Low Current		-20	uA
I_{PIH}	Input High Current		+20	uA
C_{PIN}	Input Capacitance		10	pF
C_{CLK}	PCI Clock Input Capacitance		10	pF
C_{IDSEL}	PCI Idsel Input Capacitance		8	pF

[3] At: http://www.3dlabs.com

12.2.2 Non-PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		0.5	V
V_{OH}	Output High Voltage	2.4		V
I_{IL}	Input Low Current		+10	uA
I_{IH}	Input High Current		-10	uA
I_{IHPD}	Pulldown Input High Current		250	uA
I_{ILPU}	Pullup Input Low Current		250	uA
C_{IN}	Input Capacitance		10	pF

12.3 SSTL_2 Class I Signals (DDR Memory Interface Only)

Symbol	Parameter	Min	Max	Units
VDDQ	Output Supply Voltage (VCC25)	2.25	2.75	V
VREF	Reference Voltage (VREF=0.5xVDDQ)	1.125	1.375	V
VIL	AC Input Low Voltage		VREF-350mV	V
VIH	AC Input High Voltage	VREF+350mV		V
VIL	DC Input Low Voltage	-0.5	VREF-180mV	V
VIH	DC Input High Voltage	VREF+180mV	VDDQ+0.5	V
IOL	Low Level Output Current		-16	mA
IOH	High Level Output Current		16	mA
IIL	Low Level Input Current		2	uA
IIH	High Level Input Current		2	uA
Cin	Input Capacitance		20	pF

12.4 AC Specifications

Pin Name	Capacitive Load
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN ,AGPPipeN, AGPRbfN, AGPSBA[7:0],	50pF in PCI 33 system 10pF in AGP system
All other outputs	40pF

12.4.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	15	-	ns	
T_{PHigh}	PCIClk High Time	-	-	ns	
T_{SLow}	PCIClk Low Time	-	-	ns	
T_{MCyc}	MClkin Cycle Time	8	-	ns	
T_{MHigh}	MClkin High Time	-	-	ns	
T_{MLow}	MClkin Low Time	-	-	ns	
T_{SCyc}	SClkin Cycle Time	15	-	ns	
T_{SHigh}	SClkin High Time	6	-	ns	
T_{SLow}	SClkin Low Time	6	-	ns	
T_{DCyc}	DClk Cycle Time	4	-	ns	
T_{DHigh}	DClk High Time	-	-	ns	
T_{DLow}	DClk Low Time	-	-	ns	

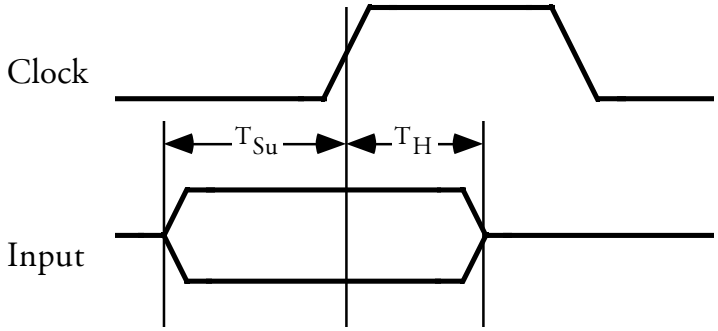


Figure 12.1 Input Timing Parameters

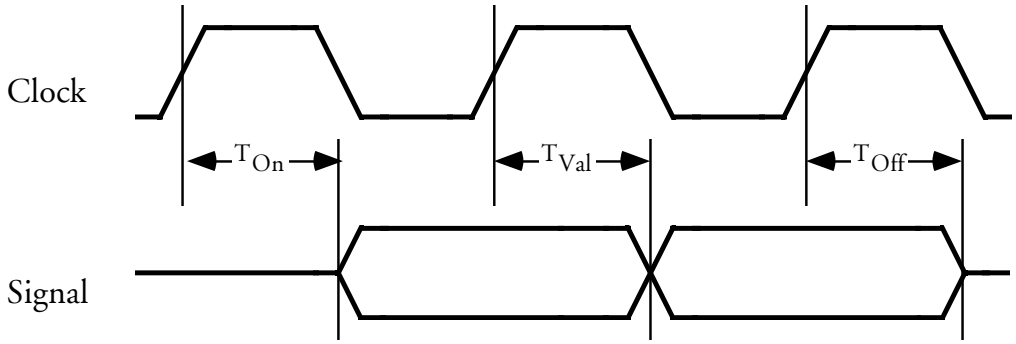


Figure 12.2 Output Timing Parameters

12.4.2 PCI Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt0-2	5	0	ns
PCIGntN	5	0	ns
PCIRstN	7	0	ns

Note: PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

12.4.3 PCI-Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}		
Parameter	Min	Max	Min	Max	Min	Max	Units
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	2	11	2	11	2	11	ns
PCIReqN	2	12					ns
PCIIntAN	2	11					ns

Note: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.4.4 AGP Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}		
Parameter	Min	Max	Min	Max	Min	Max	Units
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	1.5	6	1.5	6	1.0	14	ns
PCIReqN	1.5	6					ns
PCIIntAN	1.5	6					ns

Note: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.4.5 MEMCKOUT Referenced Input Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

Parameter	TSu Min	TH Min	Units	Notes
MDAT[63:0]	1	3	ns	

12.4.6 MEMCKOUT Referenced Output Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

	T_{Val}		T_{On}		T_{Off}			
Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
All memory control, data and address lines		8.5					ns	

13

Errata and Alerts

Alerts are part of 3Dlabs' commitment to providing comprehensive and useful information about chipset products. Alerts describe issues arising when the chip is used outside normal operating parameters and may be of interest to driver programmers.

13.1 ALERT001

13.1.1 Problem

The Delta unit has a bug relating to the way anti-aliased lines are drawn when the primitive type is a quad strip.

13.1.2 Software Workaround

Set the *AALineQuadFix* bit in the **TextureFormatControl** register. This works around the bug by sending a dummy message before each Render command.

.

13.2 R5ERN001

13.2.1 Problem

There is a DMA hanging problem in Winbench and Speedy FONT caused by (unconfirmed) the input FIFO count returning incorrect values.

13.2.2 Software Workaround

When reading a value back from the input FIFO, check to see whether it is less than 4, if it is then report that it is zero. This means that the input FIFO never actually reaches zero.

Files changed: glint.h.

13.3 R5ERN002

13.3.1 Problem

(Unconfirmed) The input FIFO count returns incorrect values

13.3.2 Software Workaround

Wait for FIFO space on R5 before starting a hostin DMA or before doing a DMA continue.

Files changed: pxrx.c

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