GLINT R4®

Reference Guide Volume IV -

Physical Characteristics

DRAFT ONLY

PROPRIETARY AND CONFIDENTIAL INFORMATION

3D*labs*®

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Issue 3

Proprietary Notice

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Change History

Document	Issue	Date	Change
160.5.4	1	06 October 99	Creation
160.5.4	2	05 December 99	R4 package description, diagram and pinlist table; thermal model draft; reset description; thermal revision and I/O pin voltages; content warning for memory, thermal and electrical chapters; inclusion of cleared Errata from P3.
160.5.4	3	31 January 2000	Added memory implementation details for *AddressExtension* field in **LocalMemControl**, video width erratum, PLL reset details

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Package Diagrams

The R4 package is a Super BGA (SBGA) with copper stiffner which conforms to JEDEC spec MO-151.

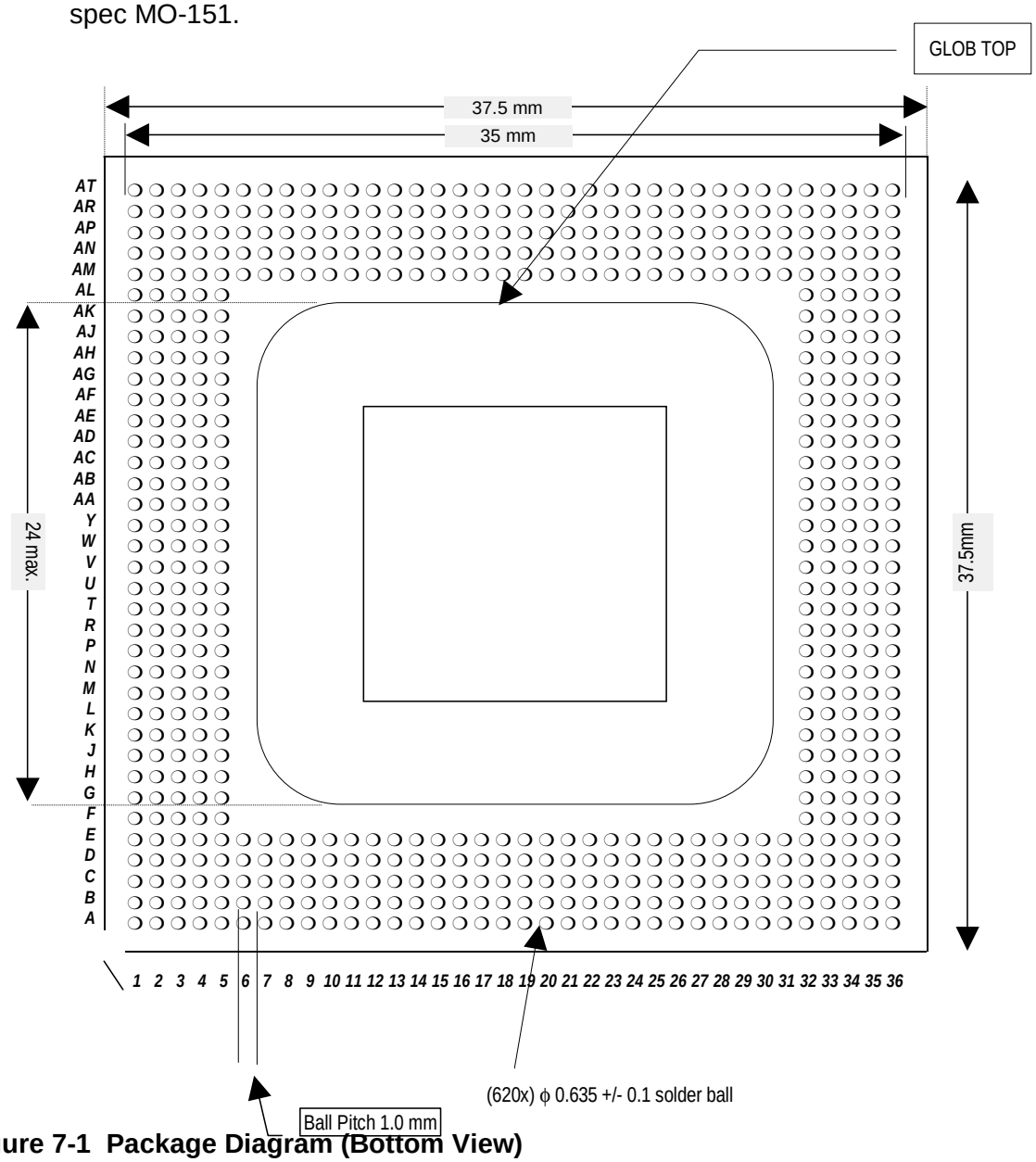

Figure 7-1 Package Diagram (Bottom View)

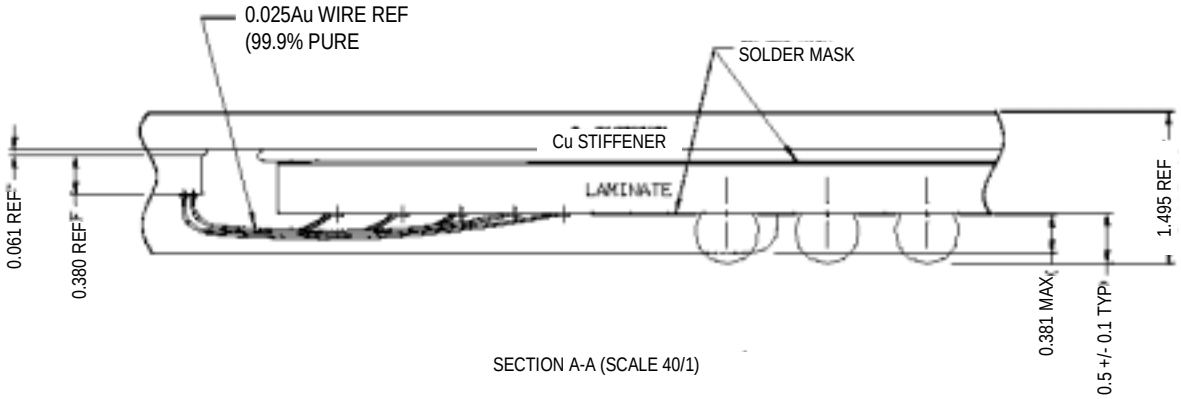

Figure 7-2 Package Diagram (Section View)

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Pin Assignment

Pin assignments are shown by pad number and by signal name. Further information on pin electrical data and use for configuration and during reset is provided in chapters 10 - *Reset* and 11 - *Electrical Characteristics*.

8.1 Pinlist by Number

The table below provides a brief description of each pin. It is organized alphabetically by pin number.

The pin type definitions used are:

I/O: Input Signal (tolerates 2.5 and 3.3 VDC PCI and AGP4X standards)

GND: Ground

VSS_3.3: Power at 3.3V

VSS_2.5: Power at 2.5 Volts

VDDQ: AGP I/O Interface voltage supplied from motherboard[1].

8.1.1 Unused AGP pins

Where AGP pins are unused, the following terminations are recommended:

AGPSBA(7:0)	No connection - output only
AGPPipeN	No connection - output only
AGPADSTB(1:0)	Tie high (input only)
AGPADSTBN(1:0)	Tie low (input only)
AGPADSTB	No connection - output only
AGPADSTBN	No connection - output only
AGPADSt(2:0)	Tie high - input only
ZSET	As per AGP termination
AGPVREF	As per AGP termination
AGPRbfN	No connection (output only)

[1] Depending on TypeDet, this will be either 1.5 or 3.3 VDC. If TypeDet is set for 3.3V signalling, then the configuration resistor AGP4Xcapable must not be set.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VDD	A01	VDD	
I/O	A10	PCICBEN0	PCI Byte Enable 0
I/O	A11	PCIAD9	PCI Address/Data line 9
I/O	A12	PCIAD11	PCI Address/Data line 11
I/O	A13	PCIAD13	PCI Address/Data line 13
I/O	A14	PCIAD15	PCI Address/Data line 15
I/O	A15	PCIAD16	PCI Address/Data line 16
I/O	A16	PCIAD18	PCI Address/Data line 18
I/O	A17	PCIAD20	PCI Address/Data line 20
I/O	A18	PCIAD22	PCI Address/Data line 22
I/O	A19	PCIAD23	PCI Address/Data line 23
VDD	A02	VDD	
I/O	A20	AGPADSTBN1	AGP AD Strobe
I/O	A21	PCIAD25	PCI Address/Data line 25
I/O	A22	PCIAD26	PCI Address/Data line 26
I/O	A23	PCIAD29	PCI Address/Data line 29
I/O	A24	PCIAD31	PCI Address/Data line 31
I/O	A25	AGPSBA7	AGP Sideband Address 7
I/O	A26	AGPSBA4	AGP Sideband Address 4
I/O	A27	AGPSBSTB	AGP Sideband Address 2X Strobe
I/O	A28	AGPSBA3	AGP Sideband Address 3
I/O	A29	AGPSBA0	AGP Sideband Address 0
I/O	A03	VIDEOMERGEHSYNCINN	Video Merge Horizontal Sync In
VDDQ	A30	VDDQ	
I/O	A31	SBGA1	SPARE
	A32	SBGA1	SPARE
	A33	SBGA1	SPARE
	A34	SBGA1	SPARE
VDD	A35	VDD	
VDD	A36	VDD	
VDDQ	A04	VDDQ	
I/O	A05	PCIAD1	PCI Address/Data line 1
I/O	A06	PCIAD3	PCI Address/Data line 3
I/O	A07	PCIAD5	PCI Address/Data line 5
I/O	A08	PCIAD7	PCI Address/Data line 7
I/O	A09	AGPADSTB0	AGP AD 2X Strobe
I/O	AA01	MADDR4	Memory Address line 4
I/O	AA02	MEMCLKOUT1	Memory Clock Output line 1
I/O	AA03	MEMCLKOUT3	Memory Clock Output line 3
I/O	AA32	VIDRIGHTEYE	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AA33	DACAGND1	
I/O	AA34	VIDRED	Analog Red signal
I/O	AA35	VIDEOMERGEDATAOUT50	Video Merge Data Output line 50
I/O	AA36	VIDEOMERGEDATAOUT54	Video Merge Data Output line 50
I/O	AA04	MADDR1	Memory Address line 1
I/O	AA05	MADDR0	Memory Address line 0
VCC	AB01	VCC3.3	
	AB02	MEMCLKOUT0	Memory Clock Output line 0
I/O	AB03	MADDR3	Memory Address line 3
VCC	AB32	VCC3.3	
I/O	AB33	VIDEOMERGEDATAOUT52	Video Merge Data Output line 52
I/O	AB34	VIDEOMERGEDATAOUT51	Video Merge Data Output line 51
I/O	AB35	VIDEOMERGEDATAOUT53	Video Merge Data Output line 53
VCC	AB36	VCC3.3	
I/O	AB04	MADDR2	Memory Address line 2
VCC	AB05	VCC3.3	
I/O	AC01	MWE	Memory Write Enable
I/O	AC02	MADDR8	Memory Address line 8
I/O	AC03	MADDR7	Memory Address line 7
	AC32	VIDEOMERGEDATAOUT57	Video Merge Data Output line 57
	AC33	VIDEOMERGEDATAOUT56	Video Merge Data Output line 56
	AC34	VIDEOMERGEDATAOUT55	Video Merge Data Output line 55
	AC35	VIDEOMERGEDATAOUT58	Video Merge Data Output line 58
	AC36	VIDEOMERGEDATAOUT62	Video Merge Data Output line 62
I/O	AC04	MADDR6	Memory Address line 6
I/O	AC05	MADDR5	Memory Address line 5
GND	AD01	GND	
I/O	AD02	MADDR11	Memory Address line 11
I/O	AD03	MADDR10	Memory Address line 10
GND	AD32	GND	
	AD33	VIDEOMERGEDATAOUT61	Video Merge Data Output line 61
	AD34	VIDEOMERGEDATAOUT60	Video Merge Data Output line 60
	AD35	VIDEOMERGEDATAOUT59	Video Merge Data Output line 59
GND	AD36	GND	
I/O	AD04	MADDR9	Memory Address line 9
GND	AD05	GND	
I/O	AE01	MCAS	Memory CAS line
I/O	AE02	MEMCLKE	Memory Clock enable
I/O	AE03	MRAS	Memory RAS line
	AE32	SBCLK	Serial Bus clock
	AE33	SBDATA	Serial Bus data

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
	AE34	VIDEOMERGECLOCKOUT	
	AE35	VIDEOMERGEDATAOUT63	Video Merge Data Output line 63
	AE36	SCLKIN	
I/O	AE04	MDSF	Memory DSF line
I/O	AE05	MEMCLKRET0	Memory Clock Return 0
VCC	AF01	VCC3.3	
	AF02	MBYTE2	Memory Byte Select 2
	AF03	MBANK1	Memory Bank Select 1
VCC	AF32	VCC3.3	
	AF33	MCLKIN	Memory Clock Input
	AF34	KCLKIN	Core Clock Input
	AF35	CLOCKIN	Merge Clock External clock Input
VCC	AF36	VCC3.3	
I/O	AF4	MBYTE1	Memory Byte Select 1
VCC	AF05	VCC3.3	
I/O	AG01	MBANK0	Memory Bank Select 0
VCC	AG02	VCC3.3	
I/O	AG03	MBYTE0	Memory Byte Select 0
I/O	AG32	XTAL2	Crystal ip 2
I/O	AG33	VIDDDCCLK	Clock line for DDC
I/O	AG34	VIDDDCDATA	Data line for DDC
VCC	AG35	VCC3.3	
I/O	AG36	ROMWEN	ROM Write Enable
I/O	AG04	MDAT11	Memory Data line 11
I/O	AG05	MDAT10	Memory Data line 10
GND	AH01	GND	
I/O	AH02	MBYTE3	Memory Byte Select 3
I/O	AH03	MDAT9	Memory Data line 9
GND	AH32	GND	
I/O	AH33	PLLDISABLE	PLL Disable
I/O	AH34	VIDVSYNC	Vertical Sync
I/O	AH35	XTAL1	Crystal ip 1
GND	AH36	GND	
I/O	AH04	MDAT13	Memory Data line 13
GND	AH05	GND	
I/O	AJ01	MBANK2	Memory Bank Select 2
GND	AJ02	GND	
I/O	AJ03	MDAT14	Memory Data line 11
I/O	AJ32	MDAT103	Memory Data line 11
I/O	AJ33	TESTSELECT0	Test Mode Select 0
I/O	AJ34	TESTSELECT2	Test Mode Select 2

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GNC	AJ35	GND	
I/O	AJ36	ROMSELECTN	ROM Select Signal
I/O	AJ04	MDAT21	Memory Data line 21
I/O	AJ05	MDAT22	Memory Data line 22
VCC	AK01	VCC3.3	
I/O	AK02	MDAT12	Memory Data line 12
I/O	AK03	MDAT20	Memory Data line 20
VCC	AK32	VCC3.3	
I/O	AK33	MDAT101	Memory Data line 101
I/O	AK34	MDAT120	Memory Data line 120
I/O	AK35	TESTMODE	Test Mode Control
VCC	AK36	VCC3.3	
I/O	AK04	MDAT18	Memory Data line 18
VCC	AK05	VCC3.3	
I/O	AL01	MDAT8	Memory Data line 8
VCC	AL02	VCC3.3	
I/O	AL03	MDAT19	Memory Data line 19
I/O	AL32	MDAT125	Memory Data line 125
I/O	AL33	MDAT100	Memory Data line 100
I/O	AL34	MDAT102	Memory Data line 102
VCC	AL35	VCC3.3	
I/O	AL36	VIDHSYNC	Horizontal Sync
I/O	AL04	MDAT16	Memory Data line 16
I/O	AL05	MDAT4	Memory Data line 4
GND	AM01	GND	
I/O	AM10	MDAT41	Memory Data line 41
VCC	AM11	VCC3.3	
I/O	AM12	MDAT51	Memory Data line 51
GND	AM13	GND	
I/O	AM14	MDAT48	Memory Data line 48
VCC	AM15	VCC3.3	
I/O	AM16	MDAT60	Memory Data line 60
GND	AM17	GND	
I/O	AM18	MBYTE11	Memory Byte Select 11
I/O	AM19	MDAT73	Memory Data line 73
I/O	AM02	MDAT23	Memory Data line 23
GND	AM20	GND	
I/O	AM21	MDAT87	Memory Data line 87
VCC	AM22	VCC3.3	
I/O	AM23	MDAT64	Memory Data line 64
GND	AM24	GND	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AM25	MDAT94	Memory Data line 94
VCC	AM26	VCC3.3	
I/O	AM27	MDAT107	Memory Data line 107
GND	AM28	GND	
I/O	AM29	MDAT112	Memory Data line 112
I/O	AM03	MDAT17	Memory Data line 117
VCC	AM30	VCC3.3	
I/O	AM31	MDAT124	Memory Data line 124
GND	AM32	GND	
I/O	AM33	MDAT122	Memory Data line 122
I/O	AM34	MDAT121	Memory Data line 121
I/O	AM35	MDAT127	Memory Data line 127
GND	AM36	GND	
I/O	AM04	MDAT6	Memory Data line 6
GND	AM05	GND	
I/O	AM06	MDAT1	Memory Data line 1
VCC	AM07	VCC3.3	
I/O	AM08	MDAT28	Memory Data line 28
GND	AM09	GND	
I/O	AN01	MDAT15	Memory Data line 15
I/O	AN10	MDAT45	Memory Data line 45
I/O	AN11	MDAT47	Memory Data line 47
I/O	AN12	MDAT52	Memory Data line 52
I/O	AN13	MDAT38	Memory Data line 38
I/O	AN14	MDAT35	Memory Data line 35
I/O	AN15	MDAT59	Memory Data line 59
I/O	AN16	MDAT61	Memory Data line 61
I/O	AN17	MBYTE9	Memory Data line 9
I/O	AN18	MDAT75	Memory Data line 75
I/O	AN19	MDAT74	Memory Data line 74
GND	AN02	GND	
I/O	AN20	MDAT79	Memory Data line 79
I/O	AN21	MDAT68	Memory Data line 68
I/O	AN22	MDAT67	Memory Data line 67
I/O	AN23	MDAT71	Memory Data line 71
I/O	AN24	MDAT88	Memory Data line 88
I/O	AN25	MDAT95	Memory Data line 95
I/O	AN26	MBYTE13	Memory Byte Select 13
I/O	AN27	MDAT106	Memory Data line 106
I/O	AN28	MDAT108	Memory Data line 108
I/O	AN29	MDAT116	Memory Data line 116

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AN03	MDAT7	Memory Data line 7
I/O	AN30	MDAT113	Memory Data line 113
I/O	AN31	MDAT96	Memory Data line 96
VDD	AN32	VDD	
VDD	AN33	VDD	
I/O	AN34	MDAT123	Memory Data line 123
GND	AN35	GND	
I/O	AN36	TESTSELECT1	Test Mode Select 1
VDD	AN04	VDD	
I/O	AN05	MDAT2	Memory Data line 2
I/O	AN06	MDAT25	Memory Data line 25
I/O	AN07	MDAT30	Memory Data line 30
I/O	AN08	MDAT31	Memory Data line 31
I/O	AN09	MBYTE4	Memory Data line 4
VCC	AP01	VCC3.3	
I/O	AP10	MDAT44	Memory Data line 44
I/O	AP11	MDAT46	Memory Data line 46
I/O	AP12	MDAT53	Memory Data line 53
I/O	AP13	MDAT39	Memory Data line 39
I/O	AP14	MDAT34	Memory Data line 34
I/O	AP15	MDAT58	Memory Data line 58
I/O	AP16	MDAT62	Memory Data line 62
I/O	AP17	MEMCLKRET2	Memory Clock Return 2
I/O	AP18	MBYTE8	Memory Byte Select 8
I/O	AP19	MDAT72	Memory Data line 72
I/O	AP02	MDAT5	Memory Data line 5
I/O	AP20	MDAT85	Memory Data line 85
I/O	AP21	MDAT86	Memory Data line 86
I/O	AP22	MDAT80	Memory Data line 80
I/O	AP23	MDAT70	Memory Data line 70
I/O	AP24	MDAT91	Memory Data line 91
I/O	AP25	MDAT92	Memory Data line 92
I/O	AP26	MBYTE14	Memory Byte Select 14
I/O	AP27	MDAT104	Memory Data line 104
I/O	AP28	MDAT111	Memory Data line 111
I/O	AP29	MDAT109	Memory Data line 109
VDD	AP03	VDD	
I/O	AP30	MDAT117	Memory Data line 117
I/O	AP31	MDAT115	Memory Data line 115
I/O	AP32	MDAT97	Memory Data line 97
I/O	AP33	MDAT99	Memory Data line 99

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VDD	AP34	VDD	
I/O	AP35	MDAT126	Memory Data line 126
VCC	AP36	VCC3.3	
I/O	AP04	MDAT3	Memory Data line 3
I/O	AP05	MDAT26	Memory Data line 26
I/O	AP06	MDAT29	Memory Data line 29
I/O	AP07	MBYTE6	Memory Byte Select 6
I/O	AP08	MEMCLKRET1	Memory Clock Return 1
I/O	AP09	MBYTE7	Memory Byte Select 7
VDD	AR01	VDD	
I/O	AR10	MDAT55	Memory Data line 55
I/O	AR11	MDAT54	Memory Data line 54
I/O	AR12	MDAT50	Memory Data line 50
I/O	AR13	MDAT36	Memory Data line 36
I/O	AR14	MDAT33	Memory Data line 33
I/O	AR15	MDAT57	Memory Data line 57
I/O	AR16	MDAT32	Memory Data line 32
I/O	AR17	MDAT56	Memory Data line 56
I/O	AR18	MDAT63	Memory Data line 63
I/O	AR19	MDAT84	Memory Data line 84
VDD	AR02	VDD	
I/O	AR20	MDAT78	Memory Data line 78
I/O	AR21	MDAT83	Memory Data line 83
I/O	AR22	MDAT81	Memory Data line 81
I/O	AR23	MDAT69	Memory Data line 69
I/O	AR24	MDAT66	Memory Data line 66
I/O	AR25	MDAT90	Memory Data line 90
I/O	AR26	MDAT93	Memory Data line 93
I/O	AR27	MEMCLKRET3	Memory Clock Return 3
VCC	AR28	VCC3.3	
I/O	AR29	MBYTE12	Memory Byte Select 12
I/O	AR003	MDAT0	Memory Data line 0
GND	AR30	GND	
I/O	AR31	MDAT110	Memory Data line 110
VCC	AR32	VCC3.3	
I/O	AR33	MDAT114	Memory Data line 114
I/O	AR34	MDAT98	Memory Data line 98
VDD	AR35	VDD	
VDD	AR36	VDD	
I/O	AR04	MDAT27	Memory Data line 27
VCC	AR05	VCC3.3	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AR06	MBYTE5	Memory Byte Select 5
GND	AR07	GND	
I/O	AR08	MDAT40	Memory Data line 11
VCC	AR09	VCC3.3	
VDD	AT01	VDD	
VCC	AT10	VCC3.3	
I/O	AT11	MDAT49	Memory Data line 49
GND	AT12	GND	
I/O	AT13	MDAT37	Memory Data line 37
VCC	AT14	VCC3.3	
I/O	AT15	VIDEOEXTCTRL	Video External Control
GND	AT16	GND	
I/O	AT17	MBYTE10	Memory Byte Select 10
I/O	AT18	RENDERSYNCN	Multi-rasterizer I/O Sync
I/O	AT19	MDAT76	Memory Data line 76
VDD	AT02	VDD	
I/O	AT20	MDAT77	Memory Data line 77
GND	AT21	GND	
I/O	AT22	MDAT82	Memory Data line 82
VCC	AT23	VCC3.3	
I/O	AT24	MDAT65	Memory Data line 65
GND	AT25	GND	
I/O	AT26	MDAT89	Memory Data line 11
VCC	AT27	VCC3.3	
I/O	AT28	MBYTE15	Memory Byte Select 15
GND	AT29	GND	
I/O	AT03	MDAT24	Memory Data line 24
I/O	AT30	MDAT105	Memory Data line 105
VCC	AT31	VCC3.3	
I/O	AT32	MDAT119	Memory Data line 119
GND	AT33	GND	
I/O	AT34	MDAT118	Memory Data line 118
VDD	AT35	VDD	
VDD	AT36	VDD	
GND	AT04	GND	
I/O	AT05	MBANK3	Memory Bank Select 3
VCC	AT06	VCC3.3	
I/O	AT07	MDAT43	Memory Data line 43
GND	AT08	GND	
I/O	AT09	MDAT42	Memory Data line 42
VDD	B01	VDD	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	B10	PCIAD8	PCI Address/Data line 8
I/O	B11	PCIAD10	PCI Address/Data line 10
I/O	B12	PCIAD12	PCI Address/Data line 12
I/O	B13	PCIAD14	PCI Address/Data line 14
I/O	B14	PCICBEN1	PCI Byte Enable 1
I/O	B15	PCICBEN2	PCI Byte Enable 2
I/O	B16	PCIAD17	PCI Address/Data line 17
I/O	B17	PCIAD19	PCI Address/Data line 19
I/O	B18	PCIAD21	PCI Address/Data line 21
I/O	B19	PCICBEN3	PCI Byte Enable 3
VDD	B02	VDD	
I/O	B20	AGPADSTB1	AGP Address Strobe 1
I/O	B21	PCIAD24	PCI Address/Data line 8
I/O	B22	PCIAD27	PCI Address/Data line 8
I/O	B23	PCIAD28	PCI Address/Data line 8
I/O	B24	PCIAD30	PCI Address/Data line 8
I/O	B25	AGPSBA6	AGP Sideband Address 6
I/O	B26	AGPSBA5	AGP Sideband Address 5
I/O	B27	AGPSBSTBN	AGP Sideband Address Strobe
I/O	B28	AGPSBA2	AGP Sideband Address 2
I/O	B29	AGPSBA1	AGP Sideband Address 1
I/O	B03	VIDEOMERGESTROBEIN	Video Merge Strobe Input
I/O	B30	AGPPIPEN	AGP Pipelined Address
I/O	B31	PCIREQN	PCI Request
I/O	B32	PCICLKSEL	33/66 MHz PCI Select[2]
I/O	B33	PCIRSTN	PCI Reset
I/O	B34	VIDEOMERGESTROBEOUT	Video Merge Strobe Output
VDD	B35	VDD	
VDD	B36	VDD	
I/O	B04	SBGA1	SPARE
I/O	B05	PCIAD0	PCI Address/Data line 8
I/O	B06	PCIAD2	PCI Address/Data line 8
I/O	B07	PCIAD4	PCI Address/Data line 8
I/O	B08	PCIAD6	PCI Address/Data line 8
I/O	B09	AGPADSTBN0	AGP Address Strobe 0
VCC	C01	VCC3.3	
	C10	SBGA1	SPARE
VDDQ	C11	VDDQ	
	C12	SBGA1	SPARE

[2] Sets (read only) bit 5 of the CFGStatus register.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
	C13	SBGA1	SPARE
	C14	SBGA1	SPARE
VDDQ	C15	VDDQ	
I/O	C16	SBGA1	SPARE
I/O	C17	SBGA1	SPARE
I/O	C18	SBGA1	SPARE
I/O	C19	SBGA1	SPARE
I/O	C02	VIDEOMERGEDATAIN5	
I/O	C20	SBGA1	SPARE
I/O	C21	SBGA1	SPARE
VDDQ	C22	VDDQ	
	C23	SBGA1	SPARE
	C24	SBGA1	SPARE
	C25	SBGA1	SPARE
VDDQ	C26	VDDQ	
	C27	SBGA1	SPARE
	C28	SBGA1	SPARE
	C29	SBGA1	SPARE
VDD	C03	VDD	
VCC	C30	VCC33	
I/O	C31	PCIINTAN	PCI Interrupt
I/O	C32	PCIFIFOINDIS	Delta Control
I/O	C33	DFPINTERRUPT	Flat Panel Interrupt line
VDD	C34	VDD	
I/O	C35	VIDEOMERGEDATAOUT1	Video Merge Data Output line 1
VCC	C36	VCC3.3	
I/O	C04	VIDEOMERGEVSYNCINN	Video Merge Vertical Sync Input
	C05	SBGA1	SPARE
	C06	SBGA1	SPARE
VDDQ	C07	VDDQ	
	C08	SBGA1	SPARE
	C09	SBGA1	SPARE
I/O	D01	VIDEOMERGEDATAIN18	Video Merge Data Input line 18
	D10	SBGA1	SPARE
	D11	SBGA1	SPARE
VCC	D12	VCC33	SPARE
I/O	D13	PCIFRAMEN	PCI Frame
I/O	D14	PCIDEVSELN	PCI Device Select
I/O	D15	PCIIRDYN	PCI Control Signal
	D16	SBGA1	SPARE
VCC	D17	VCC33	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	D18	PCIIDSEL	PCI ID Select
	D19	SBGA1	SPARE
GND	D02	GND	
	D20	SBGA1	SPARE
	D21	SBGA1	SPARE
	D22	SBGA1	SPARE
VCC	D23	VCC33	
	D24	SBGA1	SPARE
	D25	SBGA1	SPARE
	D26	SBGA1	SPARE
	D27	SBGA1	SPARE
I/O	D28	AGPRBFN	AGP Read Data Buffer Full
I/O	D29	AGPST0	AGP Status 0
I/O	D03	VIDEOMERGEDATAIN3	Video Merge Data Input line 3
I/O	D30	PCIGNTN	PCI Grant Signal
I/O	D31	PCICLK	PCI Clock
I/O	D32	DFPBLANK	Flat Panel Blank
VDD	D33	VDD	
I/O	D34	VIDEOMERGEHSYNCOUTN	
GND	D35	GND	
	D36	VIDEOMERGEDATAOUT4	Video Merge Data Output line 4
VDD	D04	VDD	
I/O	D05	TEXTUREDOWNLOADINT	Texture Download Interrupt
I/O	D06	AGPVREF	
VCC	D07	VCC33	
	D08	SBGA1	SPARE
	D09	SBGA1	SPARE
GND	E01	GND	
	E10	SBGA1	SPARE
VDD	E11	VDD	
I/O	E12	PCIPAR	PCI Ready
GND	E13	GND	
I/O	E14	PCITRDYN	PCI T Ready
VDD	E15	VDD	
	E16	SBGA1	SPARE
GND	E17	GND	
	E18	SBGA1	SPARE
	E19	SBGA1	SPARE
I/O	E2	VIDEOMERGEDATAIN13	Video Merge Data Input line 13
GND	E20	GND	
	E21	SBGA1	SPARE

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VDD	E22	VDD	
	E23	SBGA1	SPARE
GND	E24	GND	
	E25	SBGA1	SPARE
VDD	E26	VDD	
I/O	E27	AGPST2	AGP Status 2
GND	E28	GND	
I/O	E29	AGPST1	AGP Status 1
I/O	E3	VIDEOMERGEDATAIN10	Video Merge Data Input line 10
VDD	E30	VDD	
I/O	E31	PCIFIFOOUTDIS	Delta Control
GND	E32	GND	
I/O	E33	VIDEOMERGEDATAOUT0	Video Merge Data Output line 0
I/O	E34	VIDEOMERGEDATAOUT3	Video Merge Data Output line 3
I/O	E35	VIDEOMERGEDATAOUT9	Video Merge Data Output line 9
GND	E36	GND	
I/O	E4	VIDEOMERGEDATAIN1	Video Merge Data Input line 1
GND	E5	GND	
I/O	E6	ZSET	AGP interface impedance[3]
VDD	E7	VDD	
I/O	E8	PCISTOPN	PCI Stop
GND	E9	GND	
I/O	F1	VIDEOMERGEDATAIN24	Video Merge Data Input line 24
VCC	F2	VCC3.3	
I/O	F3	VIDEOMERGEDATAIN6	Video Merge Data Input line 6
I/O	F32	VIDEOMERGEVSYNCOUTN	
I/O	F33	VIDEOMERGEDATAOUT2	Video Merge Data Output line 2
I/O	F34	VIDEOMERGEDATAOUT7	Video Merge Data Output line 7
VCC	F35	VCC3.3	
I/O	F36	VIDEOMERGEDATAOUT13	Video Merge Data Output line 13
I/O	F4	VIDEOMERGEDATAIN2	Video Merge Data Input line 2
I/O	F5	VIDEOMERGEDATAIN0	Video Merge Data Input line 0
VCC	G1	VCC3.3	
I/O	G2	VIDEOMERGEDATAIN14	Video Merge Data Input line 14
I/O	G3	VIDEOMERGEDATAIN9	Video Merge Data Input line 9
VCC	G32	VCC3.3	
I/O	G33	VIDEOMERGEDATAOUT5	Video Merge Data Output line 5
I/O	G34	VIDEOMERGEDATAOUT10	Video Merge Data Output line 10
I/O	G35	VIDEOMERGEDATAOUT17	Video Merge Data Output line 17

[3] Configure using 37R5 resistor to VDDQ supply.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC	G36	VCC3.3	
	G4	VIDEOMERGEDATAIN4	Video Merge Data Input line 4
VCC	G5	VCC3.3	
I/O	H1	VIDEOMERGEDATAIN29	Video Merge Data Input line 29
GND	H2	GND	
I/O	H3	VIDEOMERGEDATAIN11	Video Merge Data Input line 11
I/O	H32	VIDEOMERGEDATAOUT6	Video Merge Data Output line 6
I/O	H33	VIDEOMERGEDATAOUT8	Video Merge Data Output line 8
I/O	H34	VIDEOMERGEDATAOUT12	Video Merge Data Output line 12
GND	H35	GND	
I/O	H36	VIDEOMERGEDATAOUT20	Video Merge Data Output line 20
I/O	H4	VIDEOMERGEDATAIN7	Video Merge Data Input line 7
I/O	H5	VIDEOMERGEDATAIN8	Video Merge Data Input line 8
GND	J1	GND	
I/O	J2	VIDEOMERGEDATAIN20	Video Merge Data Input line 20
I/O	J3	VIDEOMERGEDATAIN15	Video Merge Data Input line 15
GND	J32	GND	
I/O	J33	VIDEOMERGEDATAOUT11	Video Merge Data Output line 11
I/O	J34	VIDEOMERGEDATAOUT16	Video Merge Data Output line 16
I/O	J35	VIDEOMERGEDATAOUT21	Video Merge Data Output line 21
GND	J36	GND	
I/O	J4	VIDEOMERGEDATAIN12	Video Merge Data Input line 12
GND	J5	GND	
I/O	K1	VIDEOMERGEDATAIN33	Video Merge Data Input line 33
I/O	K2	VIDEOMERGEDATAIN22	Video Merge Data Input line 22
I/O	K3	VIDEOMERGEDATAIN19	Video Merge Data Input line 19
I/O	K32	VIDEOMERGEDATAOUT15	Video Merge Data Output line 15
I/O	K33	VIDEOMERGEDATAOUT14	Video Merge Data Output line 14
I/O	K34	VIDEOMERGEDATAOUT18	Video Merge Data Output line 18
I/O	K35	VIDEOMERGEDATAOUT25	Video Merge Data Output line 25
I/O	K36	VIDEOMERGEDATAOUT26	Video Merge Data Output line 26
I/O	K4	VIDEOMERGEDATAIN16	Video Merge Data Output line 16
I/O	K5	VIDEOMERGEDATAIN17	Video Merge Data Output line 17
VCC	L1	VCC3.3	
I/O	L2	VIDEOMERGEDATAIN27	Video Merge Data Input line 27
I/O	L3	VIDEOMERGEDATAIN23	Video Merge Data Input line 23
VCC	L32	VCC3.3	
I/O	L33	VIDEOMERGEDATAOUT19	Video Merge Data Output line 19
I/O	L34	VIDEOMERGEDATAOUT22	Video Merge Data Output line 22
I/O	L35	VIDEOMERGEDATAOUT29	Video Merge Data Output line 29
VCC	L36	VCC3.3	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	L4	VIDEOMERGEDATAIN21	Video Merge Data Input line 21
VCC	L5	VCC3.3	
I/O	M1	VIDEOMERGEDATAIN41	Video Merge Data Input line 41
I/O	M2	VIDEOMERGEDATAIN32	Video Merge Data Input line 32
I/O	M3	VIDEOMERGEDATAIN28	Video Merge Data Input line 28
I/O	M32	VIDEOMERGEDATAOUT24	Video Merge Data Output line 24
I/O	M33	VIDEOMERGEDATAOUT23	Video Merge Data Output line 23
I/O	M34	VIDEOMERGEDATAOUT28	Video Merge Data Output line 28
I/O	M35	VIDEOMERGEDATAOUT33	Video Merge Data Output line 33
I/O	M36	VIDEOMERGEDATAOUT34	Video Merge Data Output line 34
I/O	M4	VIDEOMERGEDATAIN25	Video Merge Data Input line 25
I/O	M5	VIDEOMERGEDATAIN26	Video Merge Data Input line 26
GND	N1	GND	
I/O	N2	VIDEOMERGEDATAIN37	Video Merge Data Input line 37
I/O	N3	VIDEOMERGEDATAIN31	Video Merge Data Input line 47
GND	N32	GND	
I/O	N33	VIDEOMERGEDATAOUT27	Video Merge Data Output line 27
I/O	N34	VIDEOMERGEDATAOUT30	Video Merge Data Output line 30
I/O	N35	VIDEOMERGEDATAOUT37	Video Merge Data Output line 37
GND	N36	GND	
	N4	VIDEOMERGEDATAIN30	Video Merge Data Input line 47
GND	N5	GND	
I/O	P1	VIDEOMERGEDATAIN47	Video Merge Data Input line 47
I/O	P2	VIDEOMERGEDATAIN38	Video Merge Data Input line 38
I/O	P3	VIDEOMERGEDATAIN36	Video Merge Data Input line 36
I/O	P32	VIDEOMERGEDATAOUT32	Video Merge Data Output line 32
I/O	P33	VIDEOMERGEDATAOUT31	Video Merge Data Output line 31
I/O	P34	VIDEOMERGEDATAOUT35	Video Merge Data Output line 35
I/O	P35	VIDEOMERGEDATAOUT38	Video Merge Data Output line 38
I/O	P36	VIDEOMERGEDATAOUT42	Video Merge Data Output line 42
I/O	P4	VIDEOMERGEDATAIN34	Video Merge Data Input line 34
I/O	P5	VIDEOMERGEDATAIN35	Video Merge Data Input line 35
VCC	R1	VCC3.3	
I/O	R2	VIDEOMERGEDATAIN42	Video Merge Data Input line 42
I/O	R3	VIDEOMERGEDATAIN40	Video Merge Data Input line 40
VCC	R32	VCC3.3	
I/O	R33	VIDEOMERGEDATAOUT36	Video Merge Data Output line 36
I/O	R34	VIDEOMERGEDATAOUT39	Video Merge Data Output line 39
I/O	R35	VIDEOMERGEDATAOUT44	Video Merge Data Output line 44
VCC	R36	VCC3.3	
I/O	R4	VIDEOMERGEDATAIN39	Video Merge Data Input line 39

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC	R5	VCC3.3	
I/O	T1	VIDEOMERGEDATAIN54	Video Merge Data Input line 54
I/O	T2	VIDEOMERGEDATAIN46	Video Merge Data Input line 46
I/O	T3	VIDEOMERGEDATAIN45	Video Merge Data Input line 45
I/O	T32	VIDEOMERGEDATAOUT41	Video Merge Data Output line 41
I/O	T33	VIDEOMERGEDATAOUT40	Video Merge Data Output line 40
I/O	T34	VIDEOMERGEDATAOUT43	Video Merge Data Output line 43
I/O	T35	VIDEOMERGEDATAOUT47	Video Merge Data Output line 47
I/O	T36	VIDEOMERGEDATAOUT48	Video Merge Data Output line 48
I/O	T4	VIDEOMERGEDATAIN43	Video Merge Data Input line 43
I/O	T5	VIDEOMERGEDATAIN44	Video Merge Data Output line 44
GND	U1	GND	
I/O	U2	VIDEOMERGEDATAIN50	
I/O	U3	VIDEOMERGEDATAIN49	
GND	U32	GND	
I/O	U33	VIDEOMERGEDATAOUT45	Video Merge Data Out line 45
I/O	U34	VIDEOMERGEDATAOUT46	Video Merge Data Output line 46
I/O	U35	DACFSADJ	
GND	U36	GND	
I/O	U4	VIDEOMERGEDATAIN48	
GND	U5	GND	
I/O	V1	VIDEOMERGEDATAIN60	
I/O	V2	VIDEOMERGEDATAIN55	
I/O	V3	VIDEOMERGEDATAIN51	
I/O	V32	PLLPOWER	PLL Power/Gnd Pin
I/O	V33	PLLGND	PLL Power/Gnd Pin
I/O	V34	DACAGND4	DAC power/Gnd Pin 4
I/O	V35	DACCOMP	Compensation Pin
I/O	V36	DACAVDD2	Analog/Video DAC
I/O	V4	VIDEOMERGEDATAIN52	Video Merge Data Input line 52
I/O	V5	VIDEOMERGEDATAIN53	Video Merge Data Input line 53
I/O	W1	MEMCLKOUT2	Memory Clock Output line 2
I/O	W2	VIDEOMERGEDATAIN59	Video Merge Data Input line 59
I/O	W3	VIDEOMERGEDATAIN56	Video Merge Data Input line 56
I/O	W32	DACAVDD3	Analog/Video DAC
I/O	W33	VIDBLUE	Analog Blue Signal
I/O	W34	DACAGND3	DAC Power/Gnd Pin 3
I/O	W35	VIDGREEN	Analog Green Signal
I/O	W36	DACAGND2	DAC Power/Gnd Pin 3
I/O	W4	VIDEOMERGEDATAIN57	Video Merge Data Input line 57
I/O	W5	VIDEOMERGEDATAIN58	Video Merge Data Input line 58

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	Y1	GND	
I/O	Y2	VIDEOMERGEDATAIN63	Video Merge Data Input line 63
I/O	Y3	VIDEOMERGEDATAIN61	Video Merge Data Input line 61
GND	Y32	GND	
I/O	Y33	DACAVDD1	
I/O	Y34	DACVREF	
I/O	Y35	VIDEOMERGEDATAOUT49	Video Merge Data Output line 49
GND	Y36	GND	
I/O	Y4	VIDEOMERGEDATAIN62	Video Merge Data Input line 62
GND	Y5	GND	

Table 8-1 Pinlist by Number

8.2 Pinlist by Name

The table below provides a brief description of each pin. It is organized alphabetically by pin name.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	A09	AGPADSTB0	AGP AD 2X Strobe
I/O	B20	AGPADSTB1	AGP Address Strobe 1
I/O	B09	AGPADSTBN0	AGP Address Strobe 0
I/O	A20	AGPADSTBN1	AGP AD Strobe
I/O	B30	AGPPIPEN	AGP Pipelined Address
I/O	D28	AGPRBFN	AGP Read Data Buffer Full
I/O	A29	AGPSBA0	AGP Sideband Address 0
I/O	B29	AGPSBA1	AGP Sideband Address 1
I/O	B28	AGPSBA2	AGP Sideband Address 2
I/O	A28	AGPSBA3	AGP Sideband Address 3
I/O	A26	AGPSBA4	AGP Sideband Address 4
I/O	B26	AGPSBA5	AGP Sideband Address 5
I/O	B25	AGPSBA6	AGP Sideband Address 6
I/O	A25	AGPSBA7	AGP Sideband Address 7
I/O	A27	AGPSBSTB	AGP Sideband Address 2X Strobe
I/O	B27	AGPSBSTBN	AGP Sideband Address Strobe
I/O	D29	AGPST0	AGP Status 0
I/O	E29	AGPST1	AGP Status 1
I/O	E27	AGPST2	AGP Status 2
I/O	D06	AGPVREF	
I/O	AA33	DACAGND1	
I/O	W36	DACAGND2	DAC Power/Gnd Pin 3
I/O	W34	DACAGND3	DAC Power/Gnd Pin 3
I/O	V34	DACAGND4	DAC power/Gnd Pin 4
I/O	Y33	DACAVDD1	
I/O	V36	DACAVDD2	Analog/Video DAC
I/O	W32	DACAVDD3	Analog/Video DAC
I/O	V35	DACCOMP	Compensation Pin
I/O	U35	DACFSADJ	
I/O	Y34	DACVREF	
I/O	D32	DFPBLANK	Flat Panel Blank
I/O	C33	DFPINTERRUPT	Flat Panel Interrupt line
GND	AD01	GND	
GND	AD32	GND	
GND	AD36	GND	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	AD05	GND	
GND	AH01	GND	
GND	AH32	GND	
GND	AH36	GND	
GND	AH05	GND	
GND	AJ02	GND	
GNC	AJ35	GND	
GND	AM01	GND	
GND	AM13	GND	
GND	AM17	GND	
GND	AM20	GND	
GND	AM24	GND	
GND	AM28	GND	
GND	AM32	GND	
GND	AM36	GND	
GND	AM05	GND	
GND	AM09	GND	
GND	AN02	GND	
GND	AN35	GND	
GND	AR30	GND	
GND	AR07	GND	
GND	AT12	GND	
GND	AT16	GND	
GND	AT21	GND	
GND	AT25	GND	
GND	AT29	GND	
GND	AT33	GND	
GND	AT04	GND	
GND	AT08	GND	
GND	D02	GND	
GND	D35	GND	
GND	E01	GND	
GND	E13	GND	
GND	E17	GND	
GND	E20	GND	
GND	E24	GND	
GND	E28	GND	
GND	E32	GND	
GND	E36	GND	
GND	E5	GND	
GND	E9	GND	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	H2	GND	
GND	H35	GND	
GND	J1	GND	
GND	J32	GND	
GND	J36	GND	
GND	J5	GND	
GND	N1	GND	
GND	N32	GND	
GND	N36	GND	
GND	N5	GND	
GND	U1	GND	
GND	U32	GND	
GND	U36	GND	
GND	U5	GND	
GND	Y1	GND	
GND	Y32	GND	
GND	Y36	GND	
GND	Y5	GND	
I/O	AF34	KCLKIN	Core Clock Input
I/O	AA05	MADDR0	Memory Address line 0
I/O	AA04	MADDR1	Memory Address line 1
I/O	AD03	MADDR10	Memory Address line 10
I/O	AD02	MADDR11	Memory Address line 11
I/O	AB04	MADDR2	Memory Address line 2
I/O	AB03	MADDR3	Memory Address line 3
I/O	AA01	MADDR4	Memory Address line 4
I/O	AC05	MADDR5	Memory Address line 5
I/O	AC04	MADDR6	Memory Address line 6
I/O	AC03	MADDR7	Memory Address line 7
I/O	AC02	MADDR8	Memory Address line 8
I/O	AD04	MADDR9	Memory Address line 9
I/O	AG01	MBANK0	Memory Bank Select 0
I/O	AF03	MBANK1	Memory Bank Select 1
I/O	AJ01	MBANK2	Memory Bank Select 2
I/O	AT05	MBANK3	Memory Bank Select 3
I/O	AG03	MBYTE0	Memory Byte Select 0
I/O	AF4	MBYTE1	Memory Byte Select 1
I/O	AT17	MBYTE10	Memory Byte Select 10
I/O	AM18	MBYTE11	Memory Byte Select 11
I/O	AR29	MBYTE12	Memory Byte Select 12
I/O	AN26	MBYTE13	Memory Byte Select 13

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AP26	MBYTE14	Memory Byte Select 14
I/O	AT28	MBYTE15	Memory Byte Select 15
I/O	AF02	MBYTE2	Memory Byte Select 2
I/O	AH02	MBYTE3	Memory Byte Select 3
I/O	AN09	MBYTE4	Memory Data line 4
I/O	AR06	MBYTE5	Memory Byte Select 5
I/O	AP07	MBYTE6	Memory Byte Select 6
I/O	AP09	MBYTE7	Memory Byte Select 7
I/O	AP18	MBYTE8	Memory Byte Select 8
I/O	AN17	MBYTE9	Memory Data line 9
I/O	AE01	MCAS	Memory CAS line
I/O	AF33	MCLKIN	Memory Clock Input
I/O	AR003	MDAT0	Memory Data line 0
I/O	AM06	MDAT1	Memory Data line 1
I/O	AG05	MDAT10	Memory Data line 10
I/O	AL33	MDAT100	Memory Data line 100
I/O	AK33	MDAT101	Memory Data line 101
I/O	AL34	MDAT102	Memory Data line 102
I/O	AJ32	MDAT103	Memory Data line 11
I/O	AP27	MDAT104	Memory Data line 104
I/O	AT30	MDAT105	Memory Data line 105
I/O	AN27	MDAT106	Memory Data line 106
I/O	AM27	MDAT107	Memory Data line 107
I/O	AN28	MDAT108	Memory Data line 108
I/O	AP29	MDAT109	Memory Data line 109
I/O	AG04	MDAT11	Memory Data line 11
I/O	AR31	MDAT110	Memory Data line 110
I/O	AP28	MDAT111	Memory Data line 111
I/O	AM29	MDAT112	Memory Data line 112
I/O	AN30	MDAT113	Memory Data line 113
I/O	AR33	MDAT114	Memory Data line 114
I/O	AP31	MDAT115	Memory Data line 115
I/O	AN29	MDAT116	Memory Data line 116
I/O	AP30	MDAT117	Memory Data line 117
I/O	AT34	MDAT118	Memory Data line 118
I/O	AT32	MDAT119	Memory Data line 119
I/O	AK02	MDAT12	Memory Data line 12
I/O	AK34	MDAT120	Memory Data line 120
I/O	AM34	MDAT121	Memory Data line 121
I/O	AM33	MDAT122	Memory Data line 122
I/O	AN34	MDAT123	Memory Data line 123

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AM31	MDAT124	Memory Data line 124
I/O	AL32	MDAT125	Memory Data line 125
I/O	AP35	MDAT126	Memory Data line 126
I/O	AM35	MDAT127	Memory Data line 127
I/O	AH04	MDAT13	Memory Data line 13
I/O	AJ03	MDAT14	Memory Data line 11
I/O	AN01	MDAT15	Memory Data line 15
I/O	AL04	MDAT16	Memory Data line 16
I/O	AM03	MDAT17	Memory Data line 117
I/O	AK04	MDAT18	Memory Data line 18
I/O	AL03	MDAT19	Memory Data line 19
I/O	AN05	MDAT2	Memory Data line 2
I/O	AK03	MDAT20	Memory Data line 20
I/O	AJ04	MDAT21	Memory Data line 21
I/O	AJ05	MDAT22	Memory Data line 22
I/O	AM02	MDAT23	Memory Data line 23
I/O	AT03	MDAT24	Memory Data line 24
I/O	AN06	MDAT25	Memory Data line 25
I/O	AP05	MDAT26	Memory Data line 26
I/O	AR04	MDAT27	Memory Data line 27
I/O	AM08	MDAT28	Memory Data line 28
I/O	AP06	MDAT29	Memory Data line 29
I/O	AP04	MDAT3	Memory Data line 3
I/O	AN07	MDAT30	Memory Data line 30
I/O	AN08	MDAT31	Memory Data line 31
I/O	AR16	MDAT32	Memory Data line 32
I/O	AR14	MDAT33	Memory Data line 33
I/O	AP14	MDAT34	Memory Data line 34
I/O	AN14	MDAT35	Memory Data line 35
I/O	AR13	MDAT36	Memory Data line 36
I/O	AT13	MDAT37	Memory Data line 37
I/O	AN13	MDAT38	Memory Data line 38
I/O	AP13	MDAT39	Memory Data line 39
I/O	AL05	MDAT4	Memory Data line 4
I/O	AR08	MDAT40	Memory Data line 11
I/O	AM10	MDAT41	Memory Data line 41
I/O	AT09	MDAT42	Memory Data line 42
I/O	AT07	MDAT43	Memory Data line 43
I/O	AP10	MDAT44	Memory Data line 44
I/O	AN10	MDAT45	Memory Data line 45
I/O	AP11	MDAT46	Memory Data line 46

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AN11	MDAT47	Memory Data line 47
I/O	AM14	MDAT48	Memory Data line 48
I/O	AT11	MDAT49	Memory Data line 49
I/O	AP02	MDAT5	Memory Data line 5
I/O	AR12	MDAT50	Memory Data line 50
I/O	AM12	MDAT51	Memory Data line 51
I/O	AN12	MDAT52	Memory Data line 52
I/O	AP12	MDAT53	Memory Data line 53
I/O	AR11	MDAT54	Memory Data line 54
I/O	AR10	MDAT55	Memory Data line 55
I/O	AR17	MDAT56	Memory Data line 56
I/O	AR15	MDAT57	Memory Data line 57
I/O	AP15	MDAT58	Memory Data line 58
I/O	AN15	MDAT59	Memory Data line 59
I/O	AM04	MDAT6	Memory Data line 6
I/O	AM16	MDAT60	Memory Data line 60
I/O	AN16	MDAT61	Memory Data line 61
I/O	AP16	MDAT62	Memory Data line 62
I/O	AR18	MDAT63	Memory Data line 63
I/O	AM23	MDAT64	Memory Data line 64
I/O	AT24	MDAT65	Memory Data line 65
I/O	AR24	MDAT66	Memory Data line 66
I/O	AN22	MDAT67	Memory Data line 67
I/O	AN21	MDAT68	Memory Data line 68
I/O	AR23	MDAT69	Memory Data line 69
I/O	AN03	MDAT7	Memory Data line 7
I/O	AP23	MDAT70	Memory Data line 70
I/O	AN23	MDAT71	Memory Data line 71
I/O	AP19	MDAT72	Memory Data line 72
I/O	AM19	MDAT73	Memory Data line 73
I/O	AN19	MDAT74	Memory Data line 74
I/O	AN18	MDAT75	Memory Data line 75
I/O	AT19	MDAT76	Memory Data line 76
I/O	AT20	MDAT77	Memory Data line 77
I/O	AR20	MDAT78	Memory Data line 78
I/O	AN20	MDAT79	Memory Data line 79
I/O	AL01	MDAT8	Memory Data line 8
I/O	AP22	MDAT80	Memory Data line 80
I/O	AR22	MDAT81	Memory Data line 81
I/O	AT22	MDAT82	Memory Data line 82
I/O	AR21	MDAT83	Memory Data line 83

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AR19	MDAT84	Memory Data line 84
I/O	AP20	MDAT85	Memory Data line 85
I/O	AP21	MDAT86	Memory Data line 86
I/O	AM21	MDAT87	Memory Data line 87
I/O	AN24	MDAT88	Memory Data line 88
I/O	AT26	MDAT89	Memory Data line 11
I/O	AH03	MDAT9	Memory Data line 9
I/O	AR25	MDAT90	Memory Data line 90
I/O	AP24	MDAT91	Memory Data line 91
I/O	AP25	MDAT92	Memory Data line 92
I/O	AR26	MDAT93	Memory Data line 93
I/O	AM25	MDAT94	Memory Data line 94
I/O	AN25	MDAT95	Memory Data line 95
I/O	AN31	MDAT96	Memory Data line 96
I/O	AP32	MDAT97	Memory Data line 97
I/O	AR34	MDAT98	Memory Data line 98
I/O	AP33	MDAT99	Memory Data line 99
I/O	AE04	MDSF	Memory DSF line
I/O	AE02	MEMCLKE	Memory Clock enable
I/O	AB02	MEMCLKOUT0	Memory Clock Output line 0
I/O	AA02	MEMCLKOUT1	Memory Clock Output line 1
I/O	W1	MEMCLKOUT2	Memory Clock Output line 2
I/O	AA03	MEMCLKOUT3	Memory Clock Output line 3
I/O	AE05	MEMCLKRET0	Memory Clock Return 0
I/O	AP08	MEMCLKRET1	Memory Clock Return 1
I/O	AP17	MEMCLKRET2	Memory Clock Return 2
I/O	AR27	MEMCLKRET3	Memory Clock Return 3
I/O	AE03	MRAS	Memory RAS line
I/O	AC01	MWE	Memory Write Enable
I/O	B05	PCIAD0	PCI Address/Data line 8
I/O	A05	PCIAD1	PCI Address/Data line 1
I/O	B11	PCIAD10	PCI Address/Data line 10
I/O	A12	PCIAD11	PCI Address/Data line 11
I/O	B12	PCIAD12	PCI Address/Data line 12
I/O	A13	PCIAD13	PCI Address/Data line 13
I/O	B13	PCIAD14	PCI Address/Data line 14
I/O	A14	PCIAD15	PCI Address/Data line 15
I/O	A15	PCIAD16	PCI Address/Data line 16
I/O	B16	PCIAD17	PCI Address/Data line 17
I/O	A16	PCIAD18	PCI Address/Data line 18
I/O	B17	PCIAD19	PCI Address/Data line 19

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	B06	PCIAD2	PCI Address/Data line 8
I/O	A17	PCIAD20	PCI Address/Data line 20
I/O	B18	PCIAD21	PCI Address/Data line 21
I/O	A18	PCIAD22	PCI Address/Data line 22
I/O	A19	PCIAD23	PCI Address/Data line 23
I/O	B21	PCIAD24	PCI Address/Data line 8
I/O	A21	PCIAD25	PCI Address/Data line 25
I/O	A22	PCIAD26	PCI Address/Data line 26
I/O	B22	PCIAD27	PCI Address/Data line 8
I/O	B23	PCIAD28	PCI Address/Data line 8
I/O	A23	PCIAD29	PCI Address/Data line 29
I/O	A06	PCIAD3	PCI Address/Data line 3
I/O	B24	PCIAD30	PCI Address/Data line 8
I/O	A24	PCIAD31	PCI Address/Data line 31
I/O	B07	PCIAD4	PCI Address/Data line 8
I/O	A07	PCIAD5	PCI Address/Data line 5
I/O	B08	PCIAD6	PCI Address/Data line 8
I/O	A08	PCIAD7	PCI Address/Data line 7
I/O	B10	PCIAD8	PCI Address/Data line 8
I/O	A11	PCIAD9	PCI Address/Data line 9
I/O	A10	PCICBEN0	PCI Byte Enable 0
I/O	B14	PCICBEN1	PCI Byte Enable 1
I/O	B15	PCICBEN2	PCI Byte Enable 2
I/O	B19	PCICBEN3	PCI Byte Enable 3
I/O	D31	PCICLK	PCI Clock
I/O	B32	PCICLKSEL	33/66 MHz PCI Select[4]
I/O	D14	PCIDEVSELN	PCI Device Select
I/O	C32	PCIFIFOINDIS	Delta Control
I/O	E31	PCIFIFOOUTDIS	Delta Control
I/O	D13	PCIFRAMEN	PCI Frame
I/O	D30	PCIGNTN	PCI Grant Signal
I/O	D18	PCIIDSEL	PCI ID Select
I/O	C31	PCIINTAN	PCI Interrupt
I/O	D15	PCIIRDYN	PCI Control Signal
I/O	E12	PCIPAR	PCI Ready
I/O	B31	PCIREQN	PCI Request
I/O	B33	PCIRSTN	PCI Reset
I/O	E8	PCISTOPN	PCI Stop
I/O	E14	PCITRDYN	PCI T Ready

[4] Sets (read only) bit 5 of the CFGStatus register.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AH33	PLLDISABLE	PLL Disable
I/O	V33	PLLGND	PLL Power/Gnd Pin
I/O	V32	PLLPOWER	PLL Power/Gnd Pin
I/O	AT18	RENDERSYNCN	Multi-rasterizer I/O Sync
I/O	AJ36	ROMSELECTN	ROM Select Signal
I/O	AG36	ROMWEN	ROM Write Enable
I/O	AE32	SBCLK	Serial Bus clock
I/O	AE33	SBDATA	Serial Bus data
	A31	SBGA1	SPARE
	A32	SBGA1	SPARE
	A33	SBGA1	SPARE
	A34	SBGA1	SPARE
	B04	SBGA1	SPARE
	C10	SBGA1	SPARE
	C12	SBGA1	SPARE
	C13	SBGA1	SPARE
	C14	SBGA1	SPARE
	C16	SBGA1	SPARE
	C17	SBGA1	SPARE
	C18	SBGA1	SPARE
	C19	SBGA1	SPARE
	C20	SBGA1	SPARE
	C21	SBGA1	SPARE
	C23	SBGA1	SPARE
	C24	SBGA1	SPARE
	C25	SBGA1	SPARE
	C27	SBGA1	SPARE
	C28	SBGA1	SPARE
	C29	SBGA1	SPARE
	C05	SBGA1	SPARE
	C06	SBGA1	SPARE
	C08	SBGA1	SPARE
	C09	SBGA1	SPARE
	D10	SBGA1	SPARE
	D11	SBGA1	SPARE
	D16	SBGA1	SPARE
	D19	SBGA1	SPARE
	D20	SBGA1	SPARE
	D21	SBGA1	SPARE
	D22	SBGA1	SPARE
	D24	SBGA1	SPARE

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
	D25	SBGA1	SPARE
	D26	SBGA1	SPARE
	D27	SBGA1	SPARE
	D08	SBGA1	SPARE
	D09	SBGA1	SPARE
	E10	SBGA1	SPARE
	E16	SBGA1	SPARE
	E18	SBGA1	SPARE
	E19	SBGA1	SPARE
	E21	SBGA1	SPARE
	E23	SBGA1	SPARE
	E25	SBGA1	SPARE
	AE36	SCLKIN	
I/O	AK35	TESTMODE	Test Mode Control
I/O	AJ33	TESTSELECT0	Test Mode Select 0
I/O	AN36	TESTSELECT1	Test Mode Select 1
I/O	AJ34	TESTSELECT2	Test Mode Select 2
I/O	D05	TEXTUREDOWNLOADINT	Texture Download Interrupt
VCC	AB01	VCC3.3	
VCC	AB32	VCC3.3	
VCC	AB36	VCC3.3	
VCC	AB05	VCC3.3	
VCC	AF01	VCC3.3	
VCC	AF32	VCC3.3	
VCC	AF36	VCC3.3	
VCC	AF05	VCC3.3	
VCC	AG02	VCC3.3	
VCC	AG35	VCC3.3	
VCC	AK01	VCC3.3	
VCC	AK32	VCC3.3	
VCC	AK36	VCC3.3	
VCC	AK05	VCC3.3	
VCC	AL02	VCC3.3	
VCC	AL35	VCC3.3	
VCC	AM11	VCC3.3	
VCC	AM15	VCC3.3	
VCC	AM22	VCC3.3	
VCC	AM26	VCC3.3	
VCC	AM30	VCC3.3	
VCC	AM07	VCC3.3	
VCC	AP01	VCC3.3	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC	AP36	VCC3.3	
VCC	AR28	VCC3.3	
VCC	AR32	VCC3.3	
VCC	AR05	VCC3.3	
VCC	AR09	VCC3.3	
VCC	AT10	VCC3.3	
VCC	AT14	VCC3.3	
VCC	AT23	VCC3.3	
VCC	AT27	VCC3.3	
VCC	AT31	VCC3.3	
VCC	AT06	VCC3.3	
VCC	C01	VCC3.3	
VCC	C36	VCC3.3	
VCC	F2	VCC3.3	
VCC	F35	VCC3.3	
VCC	G1	VCC3.3	
VCC	G32	VCC3.3	
VCC	G36	VCC3.3	
VCC	G5	VCC3.3	
VCC	L1	VCC3.3	
VCC	L32	VCC3.3	
VCC	L36	VCC3.3	
VCC	L5	VCC3.3	
VCC	R1	VCC3.3	
VCC	R32	VCC3.3	
VCC	R36	VCC3.3	
VCC	R5	VCC3.3	
VCC	C30	VCC33	
VCC	D12	VCC33	
VCC	D17	VCC33	
VCC	D23	VCC33	
VCC	D07	VCC33	
VDD	A01	VDD	
VDD	A02	VDD	
VDD	A35	VDD	
VDD	A36	VDD	
VDD	AN32	VDD	
VDD	AN33	VDD	
VDD	AN04	VDD	
VDD	AP03	VDD	
VDD	AP34	VDD	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VDD	AR01	VDD	
VDD	AR02	VDD	
VDD	AR35	VDD	
VDD	AR36	VDD	
VDD	AT01	VDD	
VDD	AT02	VDD	
VDD	AT35	VDD	
VDD	AT36	VDD	
VDD	B01	VDD	
VDD	B02	VDD	
VDD	B35	VDD	
VDD	B36	VDD	
VDD	C03	VDD	
VDD	C34	VDD	
VDD	D33	VDD	
VDD	D04	VDD	
VDD	E11	VDD	
VDD	E15	VDD	
VDD	E22	VDD	
VDD	E26	VDD	
VDD	E30	VDD	
VDD	E7	VDD	
VDDQ	A30	VDDQ	
VDDQ	A04	VDDQ	
VDDQ	C11	VDDQ	
VDDQ	C15	VDDQ	
VDDQ	C22	VDDQ	
VDDQ	C26	VDDQ	
VDDQ	C07	VDDQ	
I/O	W33	VIDBLUE	Analog Blue Signal
I/O	AG33	VIDDDCCLK	Clock line for DDC
I/O	AG34	VIDDDCDATA	Data line for DDC
I/O	AT15	VIDEOEXTCTRL	Video External Control
I/O	AF35	VIDEOMERGECLOCKIN	Merge Clock External clock Input
I/O	AE34	VIDEOMERGECLOCKOUT	Video Merge Clock Output
I/O	F5	VIDEOMERGEDATAIN0	Video Merge Data Input line 0
I/O	E4	VIDEOMERGEDATAIN1	Video Merge Data Input line 1
I/O	E3	VIDEOMERGEDATAIN10	Video Merge Data Input line 10
I/O	H3	VIDEOMERGEDATAIN11	Video Merge Data Input line 11
I/O	J4	VIDEOMERGEDATAIN12	Video Merge Data Input line 12
I/O	E2	VIDEOMERGEDATAIN13	Video Merge Data Input line 13

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	G2	VIDEOMERGEDATAIN14	Video Merge Data Input line 14
I/O	J3	VIDEOMERGEDATAIN15	Video Merge Data Input line 15
I/O	K4	VIDEOMERGEDATAIN16	Video Merge Data Output line 16
I/O	K5	VIDEOMERGEDATAIN17	Video Merge Data Output line 17
I/O	D01	VIDEOMERGEDATAIN18	Video Merge Data Input line 18
I/O	K3	VIDEOMERGEDATAIN19	Video Merge Data Input line 19
I/O	F4	VIDEOMERGEDATAIN2	Video Merge Data Input line 2
I/O	J2	VIDEOMERGEDATAIN20	Video Merge Data Input line 20
I/O	L4	VIDEOMERGEDATAIN21	Video Merge Data Input line 21
I/O	K2	VIDEOMERGEDATAIN22	Video Merge Data Input line 22
I/O	L3	VIDEOMERGEDATAIN23	Video Merge Data Input line 23
I/O	F1	VIDEOMERGEDATAIN24	Video Merge Data Input line 24
I/O	M4	VIDEOMERGEDATAIN25	Video Merge Data Input line 25
I/O	M5	VIDEOMERGEDATAIN26	Video Merge Data Input line 26
I/O	L2	VIDEOMERGEDATAIN27	Video Merge Data Input line 27
I/O	M3	VIDEOMERGEDATAIN28	Video Merge Data Input line 28
I/O	H1	VIDEOMERGEDATAIN29	Video Merge Data Input line 29
I/O	D03	VIDEOMERGEDATAIN3	Video Merge Data Input line 3
I/O	N4	VIDEOMERGEDATAIN30	Video Merge Data Input line 47
I/O	N3	VIDEOMERGEDATAIN31	Video Merge Data Input line 47
I/O	M2	VIDEOMERGEDATAIN32	Video Merge Data Input line 32
I/O	K1	VIDEOMERGEDATAIN33	Video Merge Data Input line 33
I/O	P4	VIDEOMERGEDATAIN34	Video Merge Data Input line 34
I/O	P5	VIDEOMERGEDATAIN35	Video Merge Data Input line 35
I/O	P3	VIDEOMERGEDATAIN36	Video Merge Data Input line 36
I/O	N2	VIDEOMERGEDATAIN37	Video Merge Data Input line 37
I/O	P2	VIDEOMERGEDATAIN38	Video Merge Data Input line 38
I/O	R4	VIDEOMERGEDATAIN39	Video Merge Data Input line 39
I/O	G4	VIDEOMERGEDATAIN4	Video Merge Data Input line 4
I/O	R3	VIDEOMERGEDATAIN40	Video Merge Data Input line 40
I/O	M1	VIDEOMERGEDATAIN41	Video Merge Data Input line 41
I/O	R2	VIDEOMERGEDATAIN42	Video Merge Data Input line 42
I/O	T4	VIDEOMERGEDATAIN43	Video Merge Data Input line 43
I/O	T5	VIDEOMERGEDATAIN44	Video Merge Data Output line 44
I/O	T3	VIDEOMERGEDATAIN45	Video Merge Data Input line 45
I/O	T2	VIDEOMERGEDATAIN46	Video Merge Data Input line 46
I/O	P1	VIDEOMERGEDATAIN47	Video Merge Data Input line 47
I/O	U4	VIDEOMERGEDATAIN48	Video Merge Data Input line 48
I/O	U3	VIDEOMERGEDATAIN49	Video Merge Data Input line 49
I/O	C02	VIDEOMERGEDATAIN5	Video Merge Data Input line 5
I/O	U2	VIDEOMERGEDATAIN50	Video Merge Data Input line 50

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	V3	VIDEOMERGEDATAIN51	Video Merge Data Input line 51
I/O	V4	VIDEOMERGEDATAIN52	Video Merge Data Input line 52
I/O	V5	VIDEOMERGEDATAIN53	Video Merge Data Input line 53
I/O	T1	VIDEOMERGEDATAIN54	Video Merge Data Input line 54
I/O	V2	VIDEOMERGEDATAIN55	Video Merge Data Input line 55
I/O	W3	VIDEOMERGEDATAIN56	Video Merge Data Input line 56
I/O	W4	VIDEOMERGEDATAIN57	Video Merge Data Input line 57
I/O	W5	VIDEOMERGEDATAIN58	Video Merge Data Input line 58
I/O	W2	VIDEOMERGEDATAIN59	Video Merge Data Input line 59
I/O	F3	VIDEOMERGEDATAIN6	Video Merge Data Input line 6
I/O	V1	VIDEOMERGEDATAIN60	Video Merge Data Input line 60
I/O	Y3	VIDEOMERGEDATAIN61	Video Merge Data Input line 61
I/O	Y4	VIDEOMERGEDATAIN62	Video Merge Data Input line 62
I/O	Y2	VIDEOMERGEDATAIN63	Video Merge Data Input line 63
I/O	H4	VIDEOMERGEDATAIN7	Video Merge Data Input line 7
I/O	H5	VIDEOMERGEDATAIN8	Video Merge Data Input line 8
I/O	G3	VIDEOMERGEDATAIN9	Video Merge Data Input line 9
I/O	E33	VIDEOMERGEDATAOUT0	Video Merge Data Output line 0
I/O	C35	VIDEOMERGEDATAOUT1	Video Merge Data Output line 1
I/O	G34	VIDEOMERGEDATAOUT10	Video Merge Data Output line 10
I/O	J33	VIDEOMERGEDATAOUT11	Video Merge Data Output line 11
I/O	H34	VIDEOMERGEDATAOUT12	Video Merge Data Output line 12
I/O	F36	VIDEOMERGEDATAOUT13	Video Merge Data Output line 13
I/O	K33	VIDEOMERGEDATAOUT14	Video Merge Data Output line 14
I/O	K32	VIDEOMERGEDATAOUT15	Video Merge Data Output line 15
I/O	J34	VIDEOMERGEDATAOUT16	Video Merge Data Output line 16
I/O	G35	VIDEOMERGEDATAOUT17	Video Merge Data Output line 17
I/O	K34	VIDEOMERGEDATAOUT18	Video Merge Data Output line 18
I/O	L33	VIDEOMERGEDATAOUT19	Video Merge Data Output line 19
I/O	F33	VIDEOMERGEDATAOUT2	Video Merge Data Output line 2
I/O	H36	VIDEOMERGEDATAOUT20	Video Merge Data Output line 20
I/O	J35	VIDEOMERGEDATAOUT21	Video Merge Data Output line 21
I/O	L34	VIDEOMERGEDATAOUT22	Video Merge Data Output line 22
I/O	M33	VIDEOMERGEDATAOUT23	Video Merge Data Output line 23
I/O	M32	VIDEOMERGEDATAOUT24	Video Merge Data Output line 24
I/O	K35	VIDEOMERGEDATAOUT25	Video Merge Data Output line 25
I/O	K36	VIDEOMERGEDATAOUT26	Video Merge Data Output line 26
I/O	N33	VIDEOMERGEDATAOUT27	Video Merge Data Output line 27
I/O	M34	VIDEOMERGEDATAOUT28	Video Merge Data Output line 28
I/O	L35	VIDEOMERGEDATAOUT29	Video Merge Data Output line 29
I/O	E34	VIDEOMERGEDATAOUT3	Video Merge Data Output line 3

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	N34	VIDEOMERGEDATAOUT30	Video Merge Data Output line 30
I/O	P33	VIDEOMERGEDATAOUT31	Video Merge Data Output line 31
I/O	P32	VIDEOMERGEDATAOUT32	Video Merge Data Output line 32
I/O	M35	VIDEOMERGEDATAOUT33	Video Merge Data Output line 33
I/O	M36	VIDEOMERGEDATAOUT34	Video Merge Data Output line 34
I/O	P34	VIDEOMERGEDATAOUT35	Video Merge Data Output line 35
I/O	R33	VIDEOMERGEDATAOUT36	Video Merge Data Output line 36
I/O	N35	VIDEOMERGEDATAOUT37	Video Merge Data Output line 37
I/O	P35	VIDEOMERGEDATAOUT38	Video Merge Data Output line 38
I/O	R34	VIDEOMERGEDATAOUT39	Video Merge Data Output line 39
	D36	VIDEOMERGEDATAOUT4	Video Merge Data Output line 4
I/O	T33	VIDEOMERGEDATAOUT40	Video Merge Data Output line 40
I/O	T32	VIDEOMERGEDATAOUT41	Video Merge Data Output line 41
I/O	P36	VIDEOMERGEDATAOUT42	Video Merge Data Output line 42
I/O	T34	VIDEOMERGEDATAOUT43	Video Merge Data Output line 43
I/O	R35	VIDEOMERGEDATAOUT44	Video Merge Data Output line 44
I/O	U33	VIDEOMERGEDATAOUT45	Video Merge Data Out line 45
I/O	U34	VIDEOMERGEDATAOUT46	Video Merge Data Output line 46
I/O	T35	VIDEOMERGEDATAOUT47	Video Merge Data Output line 47
I/O	T36	VIDEOMERGEDATAOUT48	Video Merge Data Output line 48
I/O	Y35	VIDEOMERGEDATAOUT49	Video Merge Data Output line 49
I/O	G33	VIDEOMERGEDATAOUT5	Video Merge Data Output line 5
I/O	AA35	VIDEOMERGEDATAOUT50	Video Merge Data Output line 50
I/O	AB34	VIDEOMERGEDATAOUT51	Video Merge Data Output line 51
I/O	AB33	VIDEOMERGEDATAOUT52	Video Merge Data Output line 52
I/O	AB35	VIDEOMERGEDATAOUT53	Video Merge Data Output line 53
I/O	AA36	VIDEOMERGEDATAOUT54	Video Merge Data Output line 50
I/O	AC34	VIDEOMERGEDATAOUT55	Video Merge Data Output line 55
I/O	AC33	VIDEOMERGEDATAOUT56	Video Merge Data Output line 56
I/O	AC32	VIDEOMERGEDATAOUT57	Video Merge Data Output line 57
I/O	AC35	VIDEOMERGEDATAOUT58	Video Merge Data Output line 58
I/O	AD35	VIDEOMERGEDATAOUT59	Video Merge Data Output line 59
I/O	H32	VIDEOMERGEDATAOUT6	Video Merge Data Output line 6
I/O	AD34	VIDEOMERGEDATAOUT60	Video Merge Data Output line 60
I/O	AD33	VIDEOMERGEDATAOUT61	Video Merge Data Output line 61
I/O	AC36	VIDEOMERGEDATAOUT62	Video Merge Data Output line 62
I/O	AE35	VIDEOMERGEDATAOUT63	Video Merge Data Output line 63
I/O	F34	VIDEOMERGEDATAOUT7	Video Merge Data Output line 7
I/O	H33	VIDEOMERGEDATAOUT8	Video Merge Data Output line 8
I/O	E35	VIDEOMERGEDATAOUT9	Video Merge Data Output line 9
I/O	A03	VIDEOMERGEHSYNCINN	Video Merge Horizontal Sync In

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	D34	VIDEOMERGEHSYNCOUTN	
I/O	B03	VIDEOMERGESTROBEIN	Video Merge Strobe Input
I/O	B34	VIDEOMERGESTROBEOUT	Video Merge Strobe Output
I/O	C04	VIDEOMERGEVSYNCINN	Video Merge Vertical Sync Input
I/O	F32	VIDEOMERGEVSYNCOUTN	
I/O	W35	VIDGREEN	Analog Green Signal
I/O	AL36	VIDHSYNC	Horizontal Sync
I/O	AA34	VIDRED	Analog Red signal
I/O	AA32	VIDRIGHTEYE	
I/O	AH34	VIDVSYNC	Vertical Sync
I/O	AH35	XTAL1	Crystal ip 1
I/O	AG32	XTAL2	Crystal ip 2
I/O	E6	ZSET	AGP interface impedance[5]

[5] Configure using 37R5 resistor to VDDQ supply.

9

Memory System

The GLINT R4 memory system is intended for use with Synchronous Dynamic Memories. The memories can be SGRAM or SDRAM devices. The width of the memory interface is 128 bits, but can be configured to 64 bits. Control lines are provided for 4 blocks of memories, these are Select (3 – 0). Four ClockOut and ClockReturn signals are also provided, these are to assist in de-skewing the return data and reducing the load on each clock line. The Clock lines should be wired as illustrated in Figure 9.1.

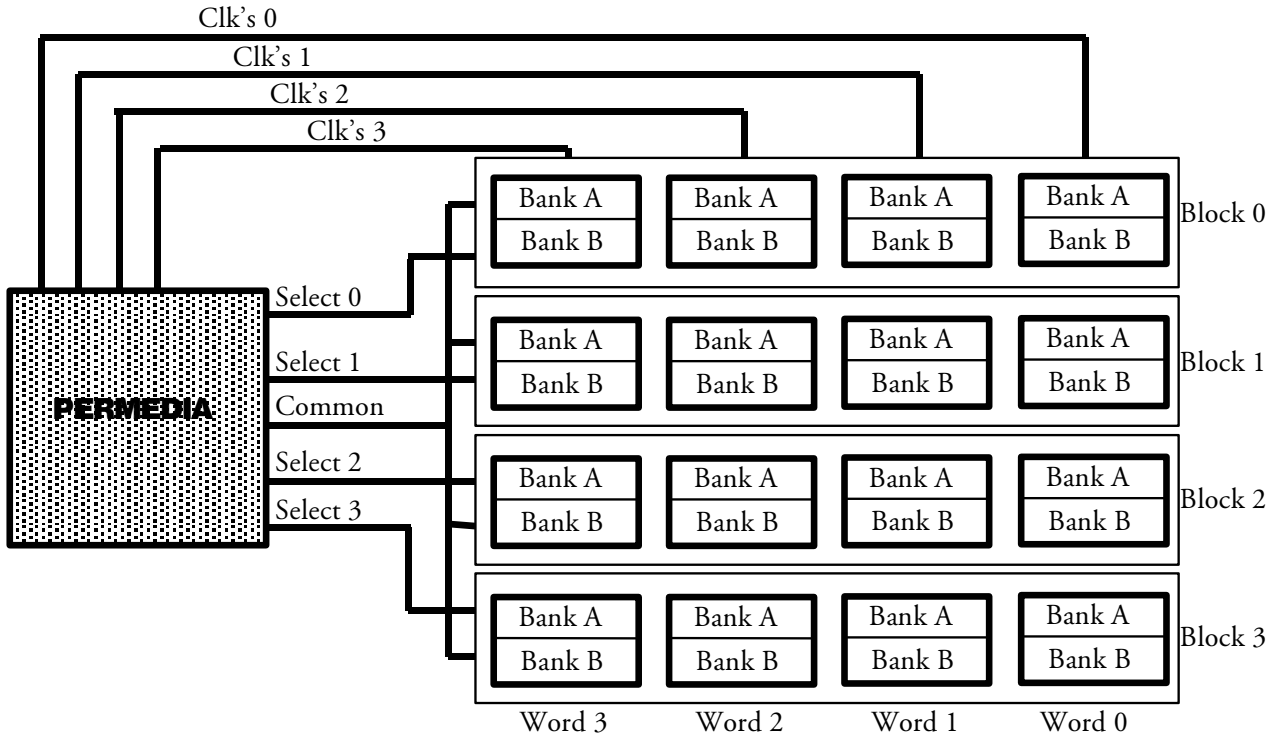

Figure 9.1 Organization of memory devices

The diagram shows a 64-megabyte memory array, constructed from 16, 32-Megabit memories, arranged into 4 blocks. The devices used are 32 bit wide with 2 banks. This layout would typically be used with SGRAMs for, e.g., CAD workstations.

To address all targeted market segments GLINT R4 supports 64 and 128 bit wide memory arrays for optimum price/performance positioning. The maximum configuration is 64Mbytes SDRAM or SGRAM, however configurations down to 2MB are supported. For a discussion of larger total memories and devices see *Using AddressExtension*, below.

- Using two 64Mbit x 32 SDRAM memory devices to give 16 Mbytes on a 64 bit bus is the cost effective, minimum part count memory organization.

- A mid-range memory organization uses four 64 Mbit x 32 SDRAM memory devices to give 32 Mbytes on a 128 bit bus.
- 64MB can be achieved using 8 x 64Mbit x 32 SDRAMS
- Four blocks of devices give 64 Mbyte configurations suitable for smaller SGRAM devices and higher performance needs, as shown above.

The memory array requires no external logic and has been designed to deliver optimum performance on low cost boards by minimizing susceptibility to signal skew.

9.1 System Parameters

The Memory System employs a rich set of registers, which allow for a diverse range of memory configurations. The various timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on memory type, speed grade and the system clock frequency (MClk). Memory functionally can be enabled depending on the type fitted. Full addressing control is available so that virtually any memory configuration can be fitted.

The following parameters are used to control accesses to the memory. These values fall into three categories

- Addressing
- Functionality and Optimizations
- Timing and Mode

9.1.1 Addressing

9.1.1.1 ColumnAddress (CAS)

This parameter defines the number of address bits required to generate the column addresses for the memory devices fitted. This parameter is normally quoted in the memory device data sheet.

For example CA7~CA0 therefore the Column Address parameter would be 8

9.1.1.2 RowAddress (RAS)

This parameter defines the number of address bits required to generate the row addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

For example RA8~RA0 therefore the Row Address parameter would be 9

9.1.1.3 BankAddress

This parameter defines the number of address bits required to generate the bank addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

For example A9(BA) therefore the Bank Address parameter would be 1

9.1.1.4 ChipSelect

This parameter defines the number of address bits needed to select all the blocks of memory devices fitted to the GLINT R4:

For 1 Block of memories	Chip Select = 1
For 2 Blocks of memories	Chip Select = 1
For 3 Blocks of memories	Chip Select = 2
For 4 Blocks of memories	Chip Select = 2

9.1.1.5 PageSize

This parameter defines the address range for a memory page of the memory array fitted. The value can be calculated as (column address bits of device – 5). The PageSize parameter is modified if either Interleave or Halfwidth are set. PageSize would then be calculated as ((column address bits)-5 + Interleave - Halfwidth).

9.1.1.6 RegionSize

This parameter defines the addressing range for each of the four page-detectors implemented in the memory controller. The minimum region a page-detector can be assigned to is one internal bank, the maximum region size is 16MB. There are some memory configurations where not all the page-detectors can be deployed. An example of this is when three blocks of memory devices are used. The value can be calculated as

Where

TotalMemory = The total size of memory fitted in

$$\mathrm{Log2}\left(\frac{\mathrm{TotalMemory}}{\mathrm{BytesperMemWidth}\times\mathrm{RegionsUsed}}\right)-5$$

megabytes

Bytes per Memory Width = 16 (128 / 8)

Regions Used =

(if total number of Banks (Blocks fitted x Internal Banks) > 4

then Blocks Fitted

else Total Banks)

For example, if the memory configuration in Figure 9-1 is constructed from sixteen 8-megabit devices each with two internal banks:

TotalMemory = 16777216 (16-megabytes)

Bytes per Memory Width = 16

Regions Used = (Blocks fitted = 4) x (Internal Banks = 2) = 8

= 8 > 4

= 4

$$\mathrm{Log2}\left(\frac{16777216}{16\times 4}\right)-5$$

RegionSize = 13

In tabular format:

Region Size	Memory fitted
15	16MB
14	8MB
13	4MB
12	2MB
11	1MB

Table 9.1 Region Sizes

9.1.1.7 InterLeave

Setting the Interleave flag doubles the page size of the memory array. This is accomplished by combining two blocks of memory and operating them as one. Both blocks are *Precharged* and *Activated* together, and any command sequences issued that cross from one block to the other do so without incurring a page break. From the example configuration detailed in Figure 9-1, Block 1 would interleave with Block 0, and Block 3 with Block 2. When this flag is set the value loaded into the PageSize parameter (9.1.1.5) should be increased by one. As the Blocks are now operating in pairs the total number of banks fitted is halved.

Note: When using InterLeave with AddressExtension the BankAddress value is incremented by 1.

9.1.1.8 HalfWidth

This flag should be set only when the memory buffer fitted is 64 bits wide. When set, this flag has an impact on the **PageSize** register, (section 9.1.1.5).

9.1.2 Using AddressExtension to control larger memory devices

GLINT R4 allows the memory controller to use bank select signals as address lines to control larger memory devices (e.g. 64MBx32 or 64MBx16). This feature is set using the *AddressExtension* field of the **LocalMemControl** register - see volume II, *Hardware Registers*, section 4.4 for information about the **LocalMemControl** register.

Note: When using InterLeave with AddressExtension the BankAddress value is incremented by 1.

Address Extension	Address Lines
0	No change
1	BankSelect0=>Address12
	BankSelect1=>BankSelect0
	BankSelect2=>BankSelect1
	BankSelect3=>BankSelect2
2	BankSelect0=>Address12

Address Extension	Address Lines
	BankSelect1=>Address13
	BankSelect2=>BankSelect0
	BankSelect3=>BankSelect1
3	BankSelect0=>Address12
	BankSelect1=>Address13
	BankSelect2=>Address14
	BankSelect3=>BankSelect0
4	BankSelect0=>Address12
	BankSelect1=>Address13
	BankSelect2=>Address14
	BankSelect3=>Address15

Table 9.2 Address Extension

For examples showing how the *AddressExtension* field can be used to configure various memory devices see section 9.2, *Example Parameter Values*.

9.1.3 Functionality and Optimizations

9.1.3.1 NoPrechargeOpt

This flag when set will disable the back to back READ - PRECHARGE optimization, inserting clocks to the value of the CAS Latency between the commands. If the memory devices fitted are capable of executing a READ command directly followed by a PRECHARGE command, this flag should be left clear for optimal performance.

9.1.3.2 SpecialModeOpt

This flag when set enables the memory controller to issue a Special Mode Register Set (SMRS) command, without regard to the current state of the internal banks of the SGRAM. Some memory devices require all internal banks to be in the same state before an SMRS command is issued. For these devices, ensure that the flag is cleared. The memory controller will issue a PRECHARGE command to the devices to ensure all internal banks are in the IDLE mode before issuing the SMRS command. If the memory devices fitted are capable of this function, optimally this flag should be set.

9.1.3.3 TwoColorBlockFill

This flag when set allows the memory controller to utilize the 2 internal Color Registers that some SGRAM devices are equipped with. If the memory devices fitted only have 1 Color Register, this flag should be cleared. When this flag is cleared the memory controller will fully emulate the two color fill operations.

9.1.3.4 NoWriteMask

This flag when set disables the memory controller from using the internal MASK Register of an SGRAM. This flag must be set if SDRAMS are fitted. When this flag is set, the memory controller will emulate the write mask operations. This is only a partial emulation using the byte enables so bit precision is not achieved.

9.1.3.5 NoBlockFill

This flag when set disables the memory controller from issuing a Block Fill command to the memories. This flag must be set if SDRAMS are fitted. When this flag is set the memory controller will fully emulate the block fill operations.

9.1.3.6 NoLookAhead

This flag when set disables the memory controller from issuing command to one bank of memory, whilst another bank is in the process of PRECHARGHING. Nominally for performance, this flag should be left cleared.

9.1.4 Timing and Mode

9.1.4.1 TurnOn (Block to Block Read Delay)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ command to one block of memory devices to a READ of another Block. (Block to Block Read Delay). Two parameters from the memory device data sheet must be used to determine what value TurnOn must be set to. The timing parameter tHZ defines the tri-state time and the parameter tLZ defines the drive time of the device. If tLZ is greater than tHZ, then this parameter can safely be set to zero.

9.1.4.2 TurnOff (Read to Write Turn around)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ and a WRITE command (Read – Write turn around). This parameter is defined in the memory device data sheet, usually as tHZ.

9.1.4.3 RegisterLoad (RL)

This parameter defines the number of MClk cycles that need to be inserted between issuing a SMRS and another command. This parameter is usually detailed in the memory device data sheet as tRSC. If tRSC is quoted including the SMRS cycle, then RegisterLoad should be calculated as tRSC (in MClk cycles) – 1.

9.1.4.4 BlockWrite (BW)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCK WRITE and another command. This parameter is usually detailed in the memory device data sheet as tBWC. If tBWC is quoted including the SMRS cycle, then BlockWrite should be calculated as tBWC (in MClk cycles) – 1.

9.1.4.5 ActivateToCommand (ATC)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a command. This parameter is usually detailed in the memory device data sheet as tRCD. If tRCD is quoted including the ACTIVATE cycle, then ActivateToCommand should be calculated as tRCD (in MClk cycles) – 1.

9.1.4.6 PrechargeToActivate (PTA)

This parameter defines the number of MClk cycles that need to be inserted between issuing a PRECHARGE and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRP. If tRP is quoted including the PRECHARGE cycle, then PreChargeToActivate should be calculated as tRP (in MClk cycles) – 1.

9.1.4.7 BlockWriteToPrecharge (BTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCKWRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tBPL (tBWR). If tBPL is quoted including the BLOCKWRITE cycle, then BlockWriteToPrecharge should be calculated as tBPL (in MClk cycles) – 1.

9.1.4.8 WriteToPrecharge (WTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a WRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRDL (tWR). If tRDL is quoted including the WRITE cycle, then WriteToPrecharge should be calculated as tRDL (in MClk cycles) – 1.

9.1.4.9 ActivateToPrecharge (ATP)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRAS. If tRAS is quoted including the ACTIVATE cycle, then ActivateToPrecharge should be calculated as tRAS (in MClk cycles) – 1.

9.1.4.10 RefreshCycle (RC)

This parameter defines the number of MClk cycles that need to be inserted between issuing a REFRESH and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRC. If tRC is quoted including the REFRESH command cycle, then RefreshCycle should be calculated as tRC (in MClk cycles) – 1.

9.1.4.11 CasLatency (CL)

This parameter determines the CAS latency expected by the memory controller. The CasLatency parameter can be loaded directly with the appropriate value from the memory device data sheet. For example, if a CAS latency of 2 is required then the CasLatency parameter should be set to 2.

9.1.4.12 Mode

This parameter defines the value of the Mode Register loaded into the SGRAM at the end of the boot sequence (see data sheet). Items to note: Burst type should be sequential, burst length should be set to one and CAS latency should be consistent with the CASLatency parameter. For devices that have a Color Register field, this should be consistent with the *TwoColorBlockFill* flag. All other bits in the Mode field should be set low.

9.1.4.13 RefreshEnable

This flag should be set for Refresh commands to be issued by the memory controller.

9.1.4.14 RefreshCount

This parameter defines the period between AUTO-REFRESH commands being issued to the synchronous memories. The count is in ((MClks/32) + 16) i.e. if RefreshCount = 1, the synchronous memories will be refreshed every 32 MClk cycles ((MClks/32)-1). For the required refresh rate, see the synchronous memory data sheet.

9.2 Example Parameter Values

The following device types and values are given as examples and should not be taken as recommendations.

9.2.1.1 Samsung KM432S2030 - 64MB x 32bit SDRAMs - two blocks (64Mbytes total) using Interleave and AddressExtension

Block0:

Wire chip address lines A10 to A0 to memory address lines A10 to A0
Wire chip address line A11 to memory BA0
Wire chip bankselect0 to memory BA1
Wire chip bankselect1 to memory CS of Block 0
Wire chip bankselect2 to memory CS of Block 1
Load **LocalMemCaps** with value 0x31F31138, which represents the parameters shown below:

Addressing Parameters	Value/Comments
LocalMemCaps	
ColumnAddress	8
RowAddress	11
BankAddress	3 (2+increment for Interleave with AddressExtension)
ChipSelect	1
PageSize	3 (log2 of 255 = 8 minus 5(log2 of 32))
RegionSize	15 (log2 of (total memory / (regions used x bytes per memory word))-5(log2 of (64MB / (4x16))-5).[6]
CombineBanks	0 (Always Off)
HalfWidth	0 = Unavailable - 128 bit
LocalMemControl	
Interleave	1 = On
AddressExtension	1 = On
Functionality Parameters	Value/Comments
NoPrechargeOpt	Preferred
SpecialModeOpt	Preferred
TwoColorBlockFill	Only 1 Color Register
NoWriteMask	1 = On (SDRAM device)
NoBlockFill	1 = On (SDRAM device)
NoLookAhead	Preferred

Table 9.3 Samsung KM432S2030

[6] Log 2 of 1MB -5 = 20-5 = 15

9.2.1.2 Samsung KM4132G112 - 64MB x 32bit SDRAMs - four blocks (64MBytes total)

Addressing Parameters	Value/Comments
LocalMemCaps	
ColumnAddress	8
RowAddress	11
BankAddress	1 (no increment)
ChipSelect	2
PageSize	4 (log2 of 255 = 8 minus 5(log2 of 64)
RegionSize	15 (log2 of (total memory / (regions used x bytes per memory word))-5(log2 of (64MB / (4x16))-5).[7]
CombineBanks	0 (Always Off)
HalfWidth	0 = Unavailable - 128 bit
LocalMemControl	
Interleave	0 = Off
AddressExtension	0 = Off
Functionality Parameters	Value/Comments
NoPrechargeOpt	1= On
SpecialModeOpt	1 = On
TwoColorBlockFill	Only 1 Color Register
NoWriteMask	1 = On (SDRAM device)
NoBlockFill	1 = On (SDRAM device)
NoLookAhead	Preferred

Table 9.4 Samsung KM4132G112 - 64MB x 32bit SDRAMs

[7] Log 2 of 1MB -5 = 20-5 = 15

9.2.1.3 Samsung KM432S2030 - 64MB x 32bit SDRAMs - one block (32MBytes total), Interleave Off

Do not fit block 1. Load **LocalMemCaps** with value 0x30E301B8, which represents the following:

Addressing Parameters	Value/Comments
LocalMemCaps	
ColumnAddress	8
RowAddress	11
BankAddress	2 (no increment)
ChipSelect	0 (set to 0 to enable rollover at end of 32MB)
PageSize	3 (log2 of 255 = 8 minus 5(log2 of 32)
RegionSize	14
CombineBanks	0 (Always Off)
HalfWidth	0 = Unavailable - 128 bit
LocalMemControl	
Interleave	0 = Off
AddressExtension	1 = On
Functionality Parameters	Value/Comments
NoPrechargeOpt	1= On
SpecialModeOpt	1 = On
TwoColorBlockFill	Only 1 Color Register
NoWriteMask	1 = On (SDRAM device)
NoBlockFill	1 = On (SDRAM device)
NoLookAhead	Preferred

Table 9.5 Samsung KM432S2030 - 64MB x 32bit SDRAMs - one block, 32MB total

9.2.1.4 Micron MT48 LC4M16 - 64MB, 4x16 bit SDRAMs - one block (64MBytes total)

Wire as for 32bit memories above. Load **LocalMemCaps** with value 0x30F302C8, which represents the following:

Addressing Parameters	Value/Comments
LocalMemCaps	
ColumnAddress	8
RowAddress	12
BankAddress	2 (no increment)
ChipSelect	0 (set to 0 to enable rollover at end of 32MB)
PageSize	3 (log2 of 255 = 8 minus 5(log2 of 32)
RegionSize	15
CombineBanks	0 (Always Off)
HalfWidth	0 = Unavailable - 128 bit
LocalMemControl	
Interleave	0 = Off
AddressExtension	1 = On
Functionality Parameters	Value/Comments
NoPrechargeOpt	1= On
SpecialModeOpt	1 = On
TwoColorBlockFill	Only 1 Color Register
NoWriteMask	1 = On (SDRAM device)
NoBlockFill	1 = On (SDRAM device)
NoLookAhead	Preferred

Table 9.6 Micron MT48 LC4M16 - 64MB x 16 bit SDRAMs - one block (64MBytes total)

10 Reset

Specific signal pins are read on the trailing edge of a reset and the values present (due to pull-ups or pull-downs) are used to initialized bits of particular registers. Most of the sampled values from the I/O pins are read into the **ChipConfig** register - for details refer to volume III. In some cases they do not - e.g. **CfgMaxLat** and **CfgMinGrant** which directly update hardware registers only.

The bus interface should use the asynchronous hard reset signal to tri-state all necessary pins, and use a re-synchronised hard reset to drive its own state-machines and registers.

During software bus reset both the bus master and the bus slave state machines continue to run. However, the Region Zero registers within the PCI bus interface are reset as will as the GP Input and Output FIFOs. Driver software must write to a PCI configuration register to disable the bus master before asserting a software reset. This ensures that the master is not trying to load the GP Input FIFO during such a reset.

Note: *When bus retries are disabled the current implementation will accept and then discard all write accesses to the GP Input FIFO — this is different from the manner in which Bypass accesses are handled. The situation only occurs if driver sofware performs a soft reset and does not check that it has completed before writing to the FIFO.]*

At chip reset the *BusMasterEnable* bit in the **CFGCommand** register must be set to allow DMA to operate.

The configuration pins are mapped to real device pins as follows:

Table 10- 1 Reset Signal Pins

Name	Pin	Description
BaseClassZero	VideoMergeDataIn(32)	1 = force PCI Bass Class Code to be zero
VGAEnable	VidRightEye	1 = internal VGA subsystem present
VGAFixed	VideoMergeDataIn (34)	1 = enable VGA fixed address decoding
RetryDisable	VideoMergeDataIn (35)	1 = disable PCI Retry using "Disconnect-Without-Data"
ShortReset	VideoMergeDataIn (36)	1 = generate short "AReset" pulse (BusReset + 64 clocks)
AGP1Xcapable	VideoMergeDataIn (37)	1 = AGP 1Xcapable
SBACapable	VideoMergeDataIn (40)	1 = AGP Sideband Addressing Capable
SubsystemFromRom	DFPBlank	1 = Load subsystem Vendor ID and SubsystemID from ROM. 0 = leave as reset values
AGP2Xcapable	VideoMergeDataIn (38)	1 = AGP 2X Capable
AGP4Xcapable	VideoMergeDataIn (39)	1 = AGP 4XCapable - this should never be set on an R4 unless 4X drivers are added

Name	Pin	Description
IndirectIOEnable	VideoMergeDataIn (42)	1 = Indirect IO accesses using BaseAddress 3 are enabled
WCEnable	VideoMergeDataIn (43)	0 = Upper half of region Zero is byte-swapped 1= Upper half of region Zero flagged internally as write-combined
PrefetchEnable	VideoMergeDataIn (44)	1 = Base Address registers 1 and 2 marked as prefetchable
Alternate DeviceID	VidExtCtrl	0 = R4 device ID is 0x000D 1 = R4 device ID is 0x0011
AutoCalEnable	VideoMergeDataIn (46)	0 = AutoCal disable 1 = AutoCal enable

A hard-wired configuration pin also exists (Table 10-2). **PCIClkSel** sets bit 5 of the **CFGStatus** register, which is Read-only.

Table 10-2 Hard Configuration Pin

Name	Pin	Description
PCIClk66	PCIClkSel	0 = up to 33MHz 1 = 66 MHz

10.1 RAMDAC Resets

RAMDAC signals are reset on either program soft resets or hard (power-on) reset, with exceptions. The following signals are reset following power-on only:

RDDClkSetup[1-4]
RDDClkControl
RDDClk0PreScale
RDDClk0FeedBackScale
RDDClk0PostScale
RDDClk1PreScale
RDDClk1FeedBackScale
RDDClk1PostScale
RDDClk2PreScale
RDDClk2FeedBackScale
RDDClk2PostScale
RDDClk3PreScale
RDDClk3FeedBackScale
RDDClk3PostScale
RDDKClkControl
RDKClkPreScale
RDKClkFeedBackScale
RDKClkPostScale
RDMClkControl
RDSClkControl
RDWClkControl
RDWClkMultiplier
RDWClkDivider

Three phase locked loops (PLLs) are included in the RAMDAC unit, dedicatd to generating DClk, WClk and KClk. The DClk PLL has four sets of control registers (e.g. **RDDclkPrescale 0-4**). The set selection is defined by two control bits from outside the unit. The reset state for the DClk PLL control regsiters are:

Register set	Frequency
0	25.057MHz
1	28.278MHz
2	Undefined
3	Undefined

The KClk PLL resets to approximately 50MHz. All figures assume a 14.31818MHz external reference. The WClk PLL derives frequencies from DClk and provides a multiplier to drive DClk remotely when (e.g.) R4 is being used in multi-rasterizer mode.

An external signal can put the PLLs into bypass mode. In this mode KClk and DClk are taken from pins and the PLLs have no effect.

Note: During Power-up resets the external frequency reference must be powered at the same time as GLINT R4 or before it, to ensure normal operation.

11

Thermal

The maximum junction temperature must be kept below Tj(max)and this can only be guaranteed by proper analysis of the operating environment and the thermal path between the die and the air surrounding it.

Data shown below are provisional for R4 pending the availability of actual test results.

11.1 Device Characteristics

These are fixed characteristics of the device and are independent of the operating environment or the characteristics of any heatsink:-

Maximum Junction Temperature	$T_{j(max)}$	= 125 °C.
Maximum Power Dissipation (provisional)	Pd(max)	= 7 Watts
Nominal memory clock frequency	f_{MClk}	= 125 MHz
Nominal core clock frequency	f_{KClk}	= 125 MHz
Junction to case resistance (provisional)	θ_{jt}	= 10°C/Watt

11.2 Thermal Model

The formula used to calculate the junction temperature (Tj) for an ambient temperature of 40° C is:

(Eq: 11-1)

$$Tj = Ta + Pd(\theta_{jt} + \theta_{cs} + \theta_{sa})$$
$$= Ta + Pd\theta_{ja}$$
$$= 40 + 7(10+1)$$
$$= 117$$

Where:

Tj = Junction temperature (°C)
Ta = Ambient temperature (°C)
Pd = Power dissipation (Watts)
θ_{jt} = Junction to top of case thermal resistance (°C/Watt)
θ_{cs} = Case to Heatsink thermal resistance (°C/Watt)
θ_{sa} = Heatsink to Air thermal resistance (°C/Watt)
θ_{ja} = Total Junction to Air thermal resistance (°C/Watt)

11.3 Cooling

GLINT R4 should not require an attached heatsink or fan when used in an ordinary office environment. If ambient temperatures are expected to routinely exceed 40° C then a heatsink may be fitted.

11.4 Operation with Heatsink

With a heatsink attached to the device the junction temperature will depend on qcs and qsa where qcs is the thermal resistance of the join between the heatsink and the case and qsa is the thermal resistance of the heatsink, which will be a function of system airflow. An ambient temperature of 50° C is assumed in the following case:

(Eq: 11-4)

Heatsink to air thermal resistance	θ_{sa}	=	9.2°C
Maximum Junction Temperature	Tj(max)	=	125°C
Ambient Temperature	Ta	=	50°C
Maximum Power Dissipation	Pd(max)	=	7 Watts
Junction to air (provisional)	θ_{ja}	=	10.0°C/Watt
Junction to case (provisional)	θ_{ja}	=	1.1 °C/Watt
Heatsink to case resistance (EG 7655 epoxy - see below)	θ_{cs}	=	1.0°C/Watt

then:

$$\theta_{sa} \leq [(125 - 50)/7] - 1.1 - 1.0$$
$$10.71 - 2.1$$
$$\leq 8.61°C/Watt.$$

In this example a heatsink must be chosen which has a thermal resistance figure of no greater than 8.61° C/Watt at an airflow matching the expected airflow in the system.

11.4.1 Heatsink Attachment

The following method has been approved for the purpose of attaching a heatsink directly onto the copper surface of the SBGA package:

Thermally conductive epoxy using either Loctite Output 315 with Loctite 7386 or type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 95% coverage of the contact area.

Typical achievable θ_{cs} using this method is 1.0 ° C/Watt

12

Electrical

This data is unchnaged from Permedia4 and included provisionally until actual data for GLINT R4 is available.

12.1 Absolute Maximum Ratings

Junction Temperature	**125°C**
Storage Temperature	-65°C to 150°C
VCC2.5 DC Supply Voltage	2.8V
VCC3.3 DC Supply Voltage	3.8V
I/O Pin Voltage with respect to GND	-0.5V to VCC3.3 + 0.5V

12.2 DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
VCC3.3	Supply Voltage	3.15	3.45	V
VCC2.5	Supply Voltage	2.25	2.75	V
LPIN	Pin Inductance		10 (sig); 8 (pwr)	nH
ICC (3V)	Power Supply Current		1	A
ICC (2.5V)	Power Supply Current		1.4	A

12.2.1 PCI Signal DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{PIL}	Input Low Voltage		0.8	V
V^{PIH}	Input High Voltage	2.0		V
V_{POL}	Output Low Voltage		0.5	V
V_{POH}	Output High Voltage	2.4		V
I_{PIL}	Input Low Current		-20	uA
I_{PIH}	Input High Current		+20	uA
C_{PIN}	Input Capacitance		10	pF
C_{CLK}	PCI Clock Input Capacitance		10	pF
C_{IDSEL}	PCI Idsel Input Capacitance		8	pF

12.2.2 Non-PCI Signal DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		0.5	V

V_{OH}	Output High Voltage	2.4		V
I_{IL}	Input Low Current		+10	uA
I_{IH}	Input High Current		-10	uA
I_{IHPD}	Pulldown Input High Current		250	uA
I_{ILPU}	Pullup Input Low Current		250	uA
C_{IN}	Input Capacitance		10	pF

12.3 AC Specifications

Pin Name	Capacitive Load
MADD[9:0]., MCAS[1:0], MDSF[1:0], MRAS[1:0], MWE[1:0].	80pF
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN ,AGPPipeN, AGPRbfN, AGPSBA[7:0],	50pF in PCI 33 system 10pF in AGP system
MBANK[3:0], MBYTE[7:0], MEMCKE, MEMCKOUT[1:0], VidDDCClk, VidDDCData, VidRightEye, VidHSYNC, VidVSYNC, RenderSyncN	50pF
MDAT[63:0].	40pF
ROMSelectN, ROMWEN, SBClk, SBData, VSCtl[7:0], VSGPChipSelectN, VSGPDataAckN, VSGPDataStrobeN, VSGPReadWriteN.	30pF

12.3.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	15	-	ns	
T_{PHigh}	PCIClk High Time	-	-	ns	
T_{SLow}	PCIClk Low Time	-	-	ns	
T_{MCyc}	MClkin Cycle Time	8	-	ns	
T_{MHigh}	MClkin High Time	-	-	ns	
T_{MLow}	MClkin Low Time	-	-	ns	
T_{SCyc}	SClkin Cycle Time	15	-	ns	
T_{SHigh}	SClkin High Time	6	-	ns	
T_{SLow}	SClkin Low Time	6	-	ns	
T_{DCyc}	DClk Cycle Time	4	-	ns	
T_{DHigh}	DClk High Time	-	-	ns	
T_{DLow}	DClk Low Time	-	-	ns	

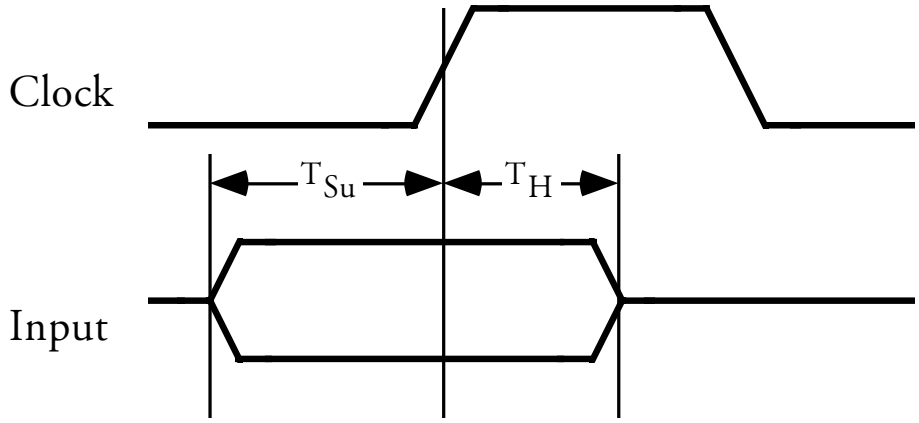

Figure 12.1 Input Timing Parameters

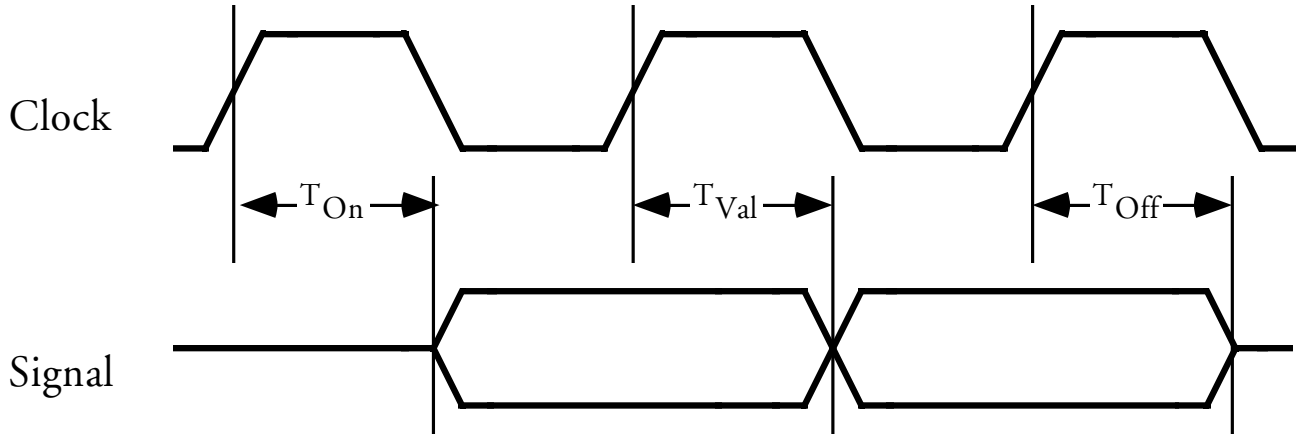

Figure 12.2 Output Timing Parameters

12.3.2 PCI Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units	Notes
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt0-2	5	0	ns	
PCIGntN	5	0	ns	
PCIRstN	7	0	ns	1

Note 1: PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

12.3.3 PCI-Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	2	11	2	11	2	11	ns	
PCIReqN	2	12					ns	
PCIIntAN	2	11					ns	1

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.3.4 AGP Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	1.5	6	1.5	6	1.0	14	ns	
PCIReqN	1.5	6					ns	
PCIIntAN	1.5	6					ns	1

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.3.5 MEMCKOUT Referenced Input Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

Parameter	**TSu Min**	**TH Min**	**Units**	**Notes**
MDAT[63:0]	1	3	ns	

12.3.6 MEMCKOUT Referenced Output Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
All memory control, data and address lines		8.5					ns	

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Errata and Alerts

Alerts are part of 3Dlabs' commitment to providing comprehensive and useful information about chipset products. Alerts describe issues arising when the chip is used outside normal operating parameters and may be of interest to driver programmers.

13.1 ALERT001 - Control DMA/ Programmed I/O Interaction Caution

13.1.1 Problem

The input fifo is not designed to cope with fast switching between Control DMA and writes to the input fifo. Normally, either one mechanism or the other (but not both) should be used. This advisory does not apply to mixing fifo/register space accesses and Hostin DMA.

13.1.2 Software Workaround

Where it is necessary to combine both write methods either (a) use HostIn DMA, or (b) ensure that the input fifo is completely empty after writing to the fifo/register space and before starting a new DMA transfer . The input FIFO must report 128 spaces available. Clamping to fewer than 128 spaces will produce unpredictable results.

13.2 ALERT002 - Texture Lockup when Cache Combining above 100MHz

13.2.1 Problem

When CombineCaches is enabled for texturing at frequencies above 100MHz, lockups may occur. When this happens check to see if the *CombineCaches* bit is set by reading back the **TextureFilterMode** register (refer to the *GLINT R4 Reference Guide*).

13.2.2 Software Workaround

Since the Primary Cache Manager is the only texture read function which uses the *CombineCaches* bit, the workaround is to ensure that drivers do not set the *CombineCaches* bit in the **TextureReadMode0/1** and **TextureFilterMode** registers if clock speeds in excess of 100MHz are anticipated.

Errata

Errata are shown with Permedia3 reference titles. Although R4 errata are not a true subset, the ability to compare functionality may be useful for programmers working with both chips. Errata which have been cleared are shown struck out - for details please refer to the *Permedia3 Errata* sheet.

13.3 PEREN001 - Video Streams

13.3.1 Problem

Operation of input and output video streams is incorrect. Modes 1, 2, 3 and 4 of the VSConfiguration register mode field do not function correctly and should not be used. Access to the ROM (mode 0) and the flat panel display (mode 6) do function correctly and can be used.

13.3.2 Software Workaround

None

~~13.4 PEREN002 - YUV Planar to Packed through bypass~~

13.5 PEREN003 - Memory frequency dependency

13.5.1 Problem

The memory and bypass clocks should not be set to run faster than the graphics processor clock. The graphics core may not function correctly if the frequency of the memory clock is greater than the frequency of the graphics processor clock. The memory clock is controlled by the MClkControl register, the bypass clock by the PclkControl register, and the graphics processor clock by KClkControl and associated PLL registers.

13.5.2 Software Workaround

Under normal conditions, the memory clock should be tied to the graphics processor clock. If slow speed memories are used, the memory clock may be run from, for example, an external clock with a frequency lower than the graphics processor clock. Care should be taken when using the power saving mode of the graphics processor clock as it may result in it having a lower frequency than the memory clock.

~~13.6 PEREN004 - Host-in DMA~~

~~13.7 PEREN005 - Video Overlay Line Length Restrictions~~

~~13.8 PEREN006 - Video Overlay de-interlacing~~

~~13.9 PEREN007 - Constant Color Spans (32bpp)~~

13.10 PEREN008 - Write DMA frequency dependency

13.10.1 Problem

The bypass write DMA controller is used to transfer data from the framebuffer to system memory. If the memory clock is operating at a higher frequency than the PCI clock, the DMA may not operate correctly. As the highest PCI clock is 66MHz, it is normal for the memory clock to be faster, so this DMA controller should not be used.

13.10.2 Software Workaround

Bypass write DMA should not be used. Instead, use the CPU to read from the framebuffer, or use the graphics processor to DMA data.

13.11 PEREN009 - GPOut write DMA

13.11.1 Problem

The **GPOutDMA** address register in region zero does not return the next DMA Address to be issued to the DMA arbiter when read. The **PCIFeedbackCount** register does not return the number of DWORDs transferred in the current DMA. This means that operations such as rectangular write DMA do not work correctly.

13.11.2 Software Workaround

Legacy output DMA, as used by PERMEDIA 2 drivers, should be used instead.

~~13.12 PEREN010 - PCI Abort Status Register~~

~~13.13 PEREN011 - GPInFifo space~~

~~13.14 PEREN012 - Video Unit Line Patching Doubling~~

~~13.15 PEREN013 - RAMDAC Pan~~

~~13.16 PEREN014 - RAMDAC Cursor~~

~~13.17 PEREN015 - Render2D Register~~

~~13.18 PEREN016 - Invalidate Texture Cache~~

13.19 PEREN017 - Display Width

The video unit imposes a 2048 pixel width constraint. Beyond this resolution the display will be wrapped.

13.19.1 Software Workaround

None.

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